PROMiS Datasheet

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Revision History

Date	Version Number	Author	Remarks
27 Dec 2012	0.1	Deepak et. al.	Draft
06 Mar 2013	0.2	Deepak et. al.	Draft
19 Apr 2013	0.3	Deepak et. al.	Draft

PROMiS IC Description

PROMiS is a (PMT Read Out Mixed Signal) chip that can read out a Photo Multiplier Tube and is optimized for single photon detection. The chip can be addressed using slow control I2C protocol. PROMiS gives the ToT information on the LVDS pins. The PMT signal is amplified and then discriminated against an adjustable threshold level. This signal is then sent as LVDS signals. The chip works on a single 3.3V supply and other electrical specifications are given in Table 1:

Features and Advantages:

1. Adjustable threshold on the comparator.
2. Separate DAC integrated to control the HV supply of the PMT.
3. Every chip can be uniquely identified (OTP).
4. Analog output capable of driving 50 Ω load.
5. Easy communication using I2C protocol.
6. Available in QFN 16 (4 mm × 4 mm) plastic package.

Applications

PMT readout.

Scintillator based applications.

Charge amplifier & discriminator.

Quick Data

	Min	Typ	Max	Remarks
VDDD & VDDA	3.0 V	3.3 V	3.6 V	
IDDD	50 mA	70 mA	90 mA	
Comp DAC	0.81 V		2.41 V	8 bits DAC
HV DAC	1.91 V		2.71 V	8 bits DAC
ID		24 bits		OTP
Operating Temperature	0 °C	40 °C	85 °C	

Table 1 PROMiS Specifications

Block Diagram

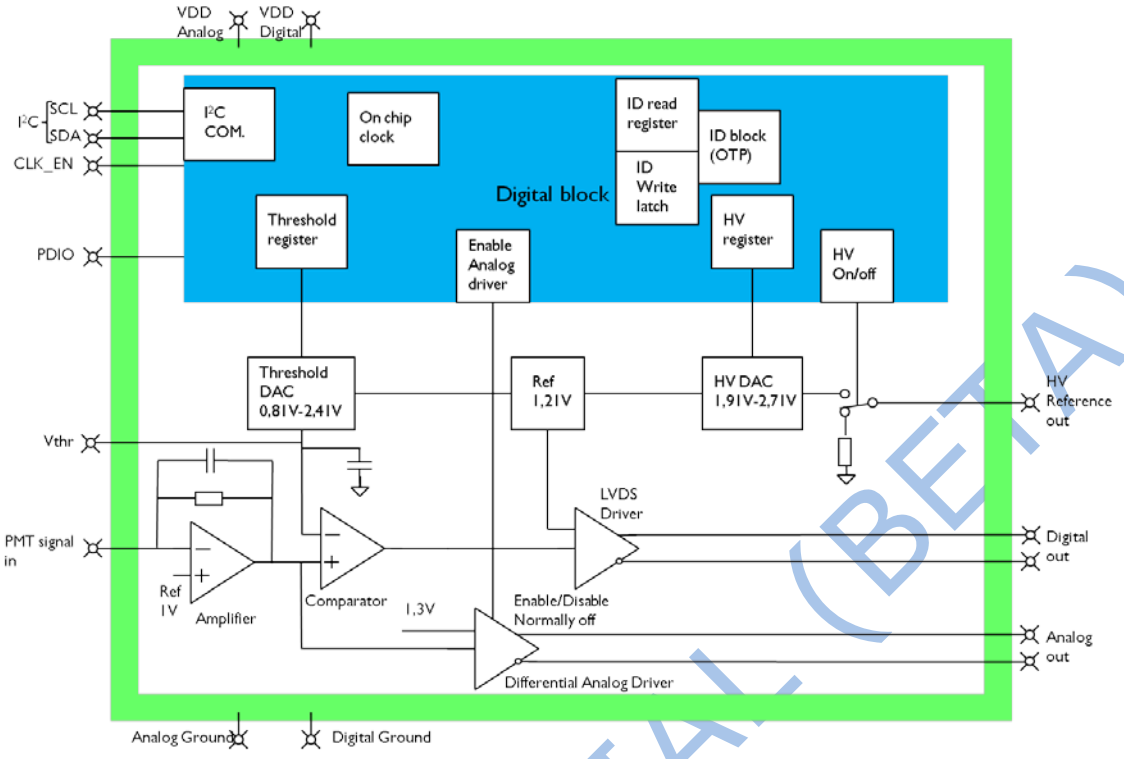


Figure 1 Block Diagram of PROMiS

Package pins configuration and description

Package pin description

PROMiS is packaged in QFN16 (with EP) 4 mm x 4 mm plastic body. Lead pitch: 0.65 mm, package height: 0.9 mm.

Pin Name	Type	Purpose	Pin No.
LVDS-	Analog Output	LVDS signal Vcm = 1.2V, Pulse width = 20ns – 300ns	1
LVDS+	Analog Output	LVDS signal Vcm = 1.2V, Pulse width = 20ns – 300ns;needs 100 Ω differential impedance w.r.t LVDSout- signal.	2
GNDD	Digital Ground	Digital Ground	3
Vthr	Analog Output	Threshold voltage, DC, 810mV - 2.41V in 256 steps	4

In_preamp	Analog Input	Analog signal Tr = 2ns, Ampl = 50mV – 500mV in series with 3.3pF capacitor	5
GNDA	Analog Ground	Analog Ground	6
VDDA	Analog Power	Analog Power (80mA max.)	7
HVDACOUT	Analog Output	Analog Signal 1.91 V - 2.71 V in 256 steps	8
PDIO	Digital IO	OTP block program port	9
SDA	Digital IO	I2C Data signal at 250 kHz or 400 kHz	10
SCL	Digital IO	I2C Clock signal at 250 kHz or 400 kHz	11
Clk_enable	Digital Input	Clock enable for the on chip clock generator	12
VDDD	Digital Power	Digital Power (30 mA max.)	13
GNDD	Digital Ground	Digital Ground	14
Anabuf+	Analog Output	Analog differential signal Tr = 2ns, Ampl = 1.0V – 3.3V; internal termination present.	15
Anabuf-	Analog Output	Analog differential signal Tr = 2ns, Ampl = 1.0V – 3.3V; internal termination present	16

Table 2: Package pin description

Absolute Maximum Ratings

Symbol	Pin	Parameter	Min	Max	Unit
LVDS	1,2	Low voltage differential signaling	0.8	1.6	V
Vthr	4	Comparator threshold voltage	0.75	2.45	V
In_preamp	5	Pre-amplifier input	0	3.3	V
VDD(D)(A)	7,13	Supply voltage	3.0	3.6	V
HVDAC	8	Digital to analog converter	1.85	2.8	V
Digital I/O	9 to 12	Digital Inputs and outputs	3.0	3.3	V

Anabuf	15,16	Analog Buffer	1.5	3.3	V
P_D		Total Power Dissipation	0.04	0.25	W
T_j		Junction temperature	0	85	°C

Table 3: Absolute Maximum Rating

Electrical Specifications

All specifications/characteristics are at 3.3 V supply and T = 25 °C unless otherwise specified.

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
IC Supply Voltage						
VDD	Operating range	Device operational	3.0	3.3	3.6	V
Supply Current						
Iq	Quiescent current	Device on, Standby		4	4.5	mA
Iop	Operational current	Device on, Clock off		7	9	mA
Iop	Operational current	Device on, Clock running		7	10	mA
Iop	Operational current	Device on, Analog Buffer on	65		70	mA
Input Stage						
Cin	Input charge	Device on	128	160	800	fC
Trise	Rise time of the signal	Device operational	1	2		ns
Output LVDS Stage						
ToT	Time over threshold	Single photoelectron charge	15	19	23	ns
Trise	Rise time of the signal	Single photoelectron charge	2			ns
Output Analog Buffer						
Vbuf	Amplitude of the analog pulse	Single photoelectron charge	300	350	400	mV

Trise	Rise time of the signal	Single photoelectron charge	2			ns
Comparator Threshold						
Vthr	Threshold value of the comparator	Device startup	0.795	0.8	0.805	V
Treac	Reaction time of the DAC	Device operational	50	75	100	µs
Vthr	Operational range of the comparator	Device operational	0.8		2.4	V
DAC used for HV setting						
HVDAC	Output of the DAC	Device startup	0.05	0	0.2	V
Treac	Reaction time of the DAC	Device operational	50	75	100	µs
HVDAC	Operational range of the HVDAC	Device operational	1.9		2.7	V
Digital Block						
Power on Reset block						
Tpor	Time to reset	Device power up		2.5		µs
Vpor	Voltage threshold for POR	Device power up		2		V
Internal Clock						
Freq.	Internal clock frequency	Device operational and clk_enable = 1	9	10	11	MHz
I2C Slave block						
Freq.	I2C clock frequency	Device operational and clk_enable = 1	100	250	400	kHz
OTP (To uniquely identify each chip)						
Bits	One time programmable memory			24		Bits

Table 4: Absolute Maximum Rating

Typical Performance Graphs

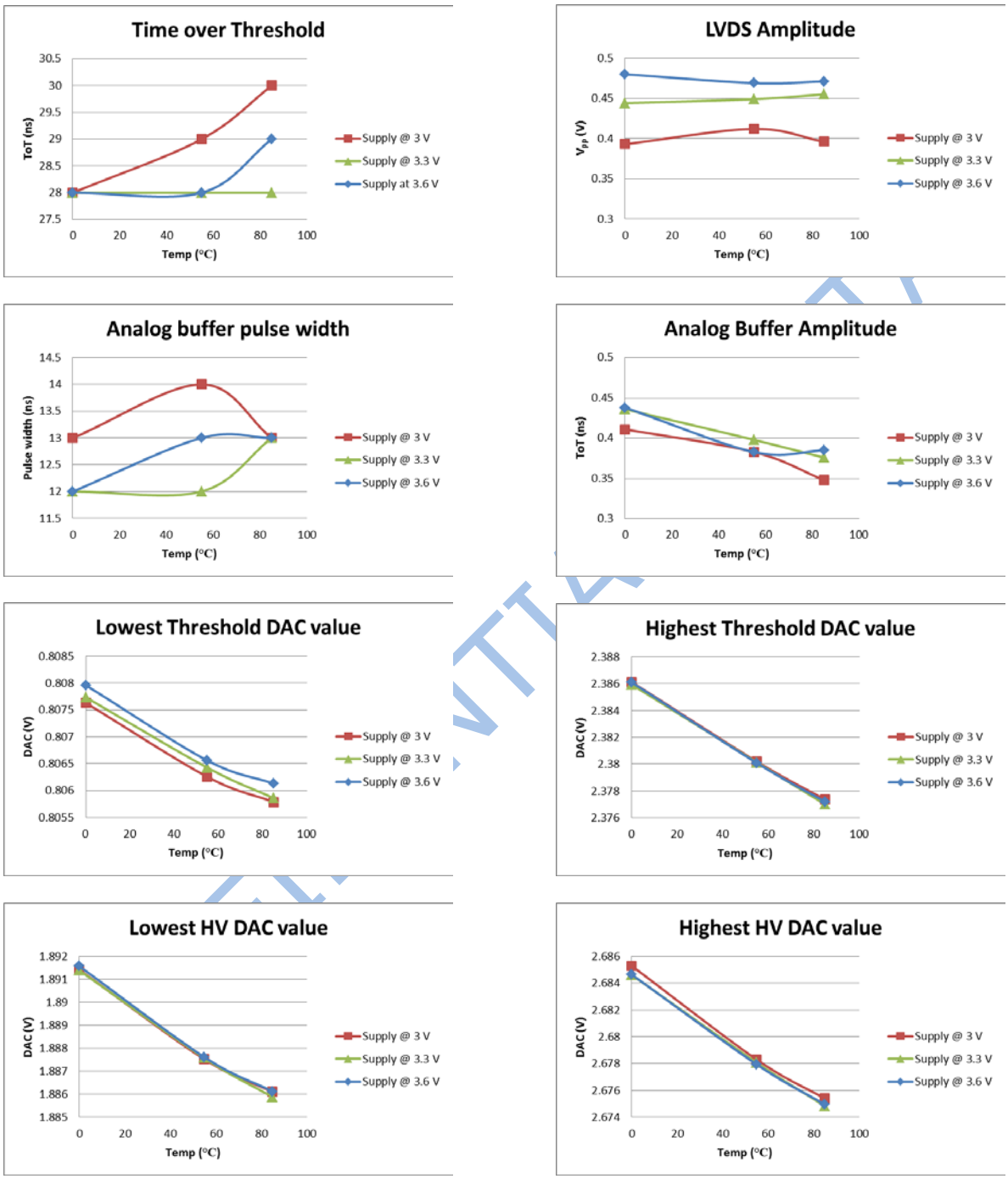


Figure 2 Typical Performance characteristics depending on temperature and power supply variations.

Functionality description

Digital Part

All digital blocks are supplied by VDDD. This is to separate all switching currents and noise from the sensitive analog blocks.

Power On Reset

During every power up sequence, a reset signal is issued and all registers and digital blocks are reset to their default values. It sets the 24 bit memory in auto-read mode.

Clock Generator

An on chip clock generator (with an enable signal) for the digital block has been implemented. The clock runs at 10 MHz. The clock may be disabled to save power. This clock is utilized by the I^2C block to sample the I^2C SCL clock line and the digital control blocks.

OTP (One Time Programmable memory)

An one time field programmable memory (24 bits) is integrated. It is meant to give each chip an unique ID. It does not need a separate voltage for programming. The burning process is implemented as a simple I^2C sequence.

I^2C slave block

The slow control of PROMiS ASIC is done via I^2C (http://en.wikipedia.org/wiki/I%C2%B2C). The PROMiS acts as a slave only with its 7 bit address “0110000”. There are 16 registers with HEX pointers ranging from 0x0 until 0xF, of which, only 11 are accessible. Following is the write and read format of the I^2C registers. (Also shown in Table 5)

Pointer 0 – Comparator Threshold register , threshold level of comparator can be set.

Pointer 1 – High Voltage DAC register, the desired level of high voltage can be set.

Pointer 2 - Control register, a few analog/digital functionality of the chip can be controlled.

Pointer 3 – Reserved.

Pointer 4 – Desired ID data register, Lowest byte of the desired ID to be written in the latch of OTP.

Pointer 5 – Desired ID data register, Middle byte of the desired ID to be written in the latch of OTP.

Pointer 6 – Desired ID data register, Highest byte of the desired ID to be written in the latch of OTP.

These 3 bytes will be burnt finally in the One Time Programmable memory – (OTP) also called PROM.

Pointer 7 – Reserved.

Pointer 8 (Read only) – Actual ID/ Burnt data of OTP/PROM, Lowest byte of the ID .

Pointer 9 (Read only) – Actual ID/ Burnt data of OTP/PROM, Middle byte of the ID.

Pointer 10 (Read only) – Actual ID/ Burnt data of OTP/PROM, Highest byte of the ID.

For example, if we would like to address the HVDAC register, then we first address the PROMiS ASIC by its 7 bit slave address “0110000” and then Pointer 1 and then the data for the comparator threshold register. The pointer is automatically incremented. The next data byte (if supplied) is written into Pointer 2. We can either choose to stop the I^2C protocol here or go on by issuing a repeated start condition of I^2C.

Write	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pointer 0	Cmprtr Threshold 7	Cmprtr Threshold 6	Cmprtr Threshold 5	Cmprtr Threshold 4	Cmprtr Threshold 3	Cmprtr Threshold 2	Cmprtr Threshold 1	Cmprtr Threshold 0
Pointer 1	HV DAC 7	HV DAC 6	HV DAC 5	HV DAC 4	HV DAC 3	HV DAC 2	HV DAC 1	HV DAC 0
Pointer 2	NC	Ana_buf_on_off	PROM burn	100mA OK	Analog Chain Test	HV_on_off	Latch Write	PROM Read
Pointer 3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Pointer 4	PROG data 7	PROG data 6	PROG data 5	PROG data 4	PROG data 3	PROG data 2	PROG data 1	PROG data 0
Pointer 5	PROG data 15	PROG data 14	PROG data 13	PROG data 12	PROG data 11	PROG data 10	PROG data 9	PROG data 8
Pointer 6	PROG data 23	PROG data 22	PROG data 21	PROG data 20	PROG data 19	PROG data 18	PROG data 17	PROG data 16
Read	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Pointer 0	Cmprtr Threshold 7	Cmprtr Threshold 6	Cmprtr Threshold 5	Cmprtr Threshold 4	Cmprtr Threshold 3	Cmprtr Threshold 2	Cmprtr Threshold 1	Cmprtr Threshold 0
Pointer 1	HV DAC 7	HV DAC 6	HV DAC 5	HV DAC 4	HV DAC 3	HV DAC 2	HV DAC 1	HV DAC 0
Pointer 2	NC	Ana_buf_on_off	PROM burn	100mA OK	Analog Chain Test	HV_on_off	Latch Write	PROM Read

Pointer 3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Pointer 4	PROG data 7	PROG data 6	PROG data 5	PROG data 4	PROG data 3	PROG data 2	PROG data 1	PROG data 0
Pointer 5	PROG data 15	PROG data 14	PROG data 13	PROG data 12	PROG data 11	PROG data 10	PROG data 9	PROG data 8
Pointer 6	PROG data 23	PROG data 22	PROG data 21	PROG data 20	PROG data 19	PROG data 18	PROG data 17	PROG data 16
Pointer 7	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Pointer 8	PROM data 7	PROM data 6	PROM data 5	PROM data 4	PROM data 3	PROM data 2	PROM data 1	PROM data 0
Pointer 9	PROM data 15	PROM data 14	PROM data 13	PROM data 12	PROM data 11	PROM data 10	PROM data 9	PROM data 8
Pointer 10	PROM data 23	PROM data 22	PROM data 21	PROM data 20	PROM data 19	PROM data 18	PROM data 17	PROM data 16

Table 5: I2C registers for I2C communication.

Analog Part

All bias currents and reference voltages needed are derived from a stable reference voltage of the Bandgap block. Sensitive analog blocks like Preamplifier and comparator are supplied by a separate line VDDA.

Preamplifier

Preamplifier has a fixed RC ~ 4.5 ns feedback. It is meant to be used as a charge amplifier. The preamplifier is biased at 1.0 V. So, the threshold of the comparator (next stage) should be above 1.0 V.

Comparator

The comparator compares the pre-amplified signal with an adjustable threshold value. The threshold for the comparator can be adjusted between 0.8 V and 2.4 V in 256 steps. The value for the DAC can be set using I^2C register (Poniter 0).

LVDS

The Time over Threshold (ToT) is converted to a standard LVDS (Low Voltage Differential Signal) format.

Analog Buffer

The output of the preamplifier is made available as a differential output. The buffer can drive 50 Ω load.

Comparator DAC

The threshold of the comparator is adjustable. A simple Kelvin-Varley divider based 8 bit DAC is included in the chip. The dynamic range of the DAC is set from 0.8 V to 2.4 V in 256 steps. The step size is calculated to be 6.25 mV. The value of this DAC can be set in Register 0.

HVDAC

An extra DAC is integrated in the chip to adjust the HV needed for the PMT. A simple Kelvin-Varley divider based 8 bit DAC is included in the chip. The dynamic range of the DAC is set from 1.9 V to 2.7 V in 256 steps. The step size is calculated to be 3.125 mV. The value of this DAC can be set in Register 1.

Typical Application and Layout Guidelines

The board needs a single 3.3 V supply. The chip has two supplies for the digital and analog blocks. For test purposes, these supplies can be combined to a single supply.

All capacitors are NP0 type (unless otherwise specified), all resistors are rated with 1% tolerance.

PIN10 and PIN11 are I^2C communication ports. They need a pull up of 4.7 kΩ to the 3V3 PWR supply.

PIN1 and PIN2 are LVDS signals (Common mode: 1.2 V). It needs a differential 100 Ω resistor between them.

PIN15 and PIN16 are differential analog buffer signals (Common mode: 1.65 V). These can be tested by blocking the DC with a 100nF capacitor and then terminating it with a 50 Ω load.

A typical PMT Base application is shown in Figure 3.

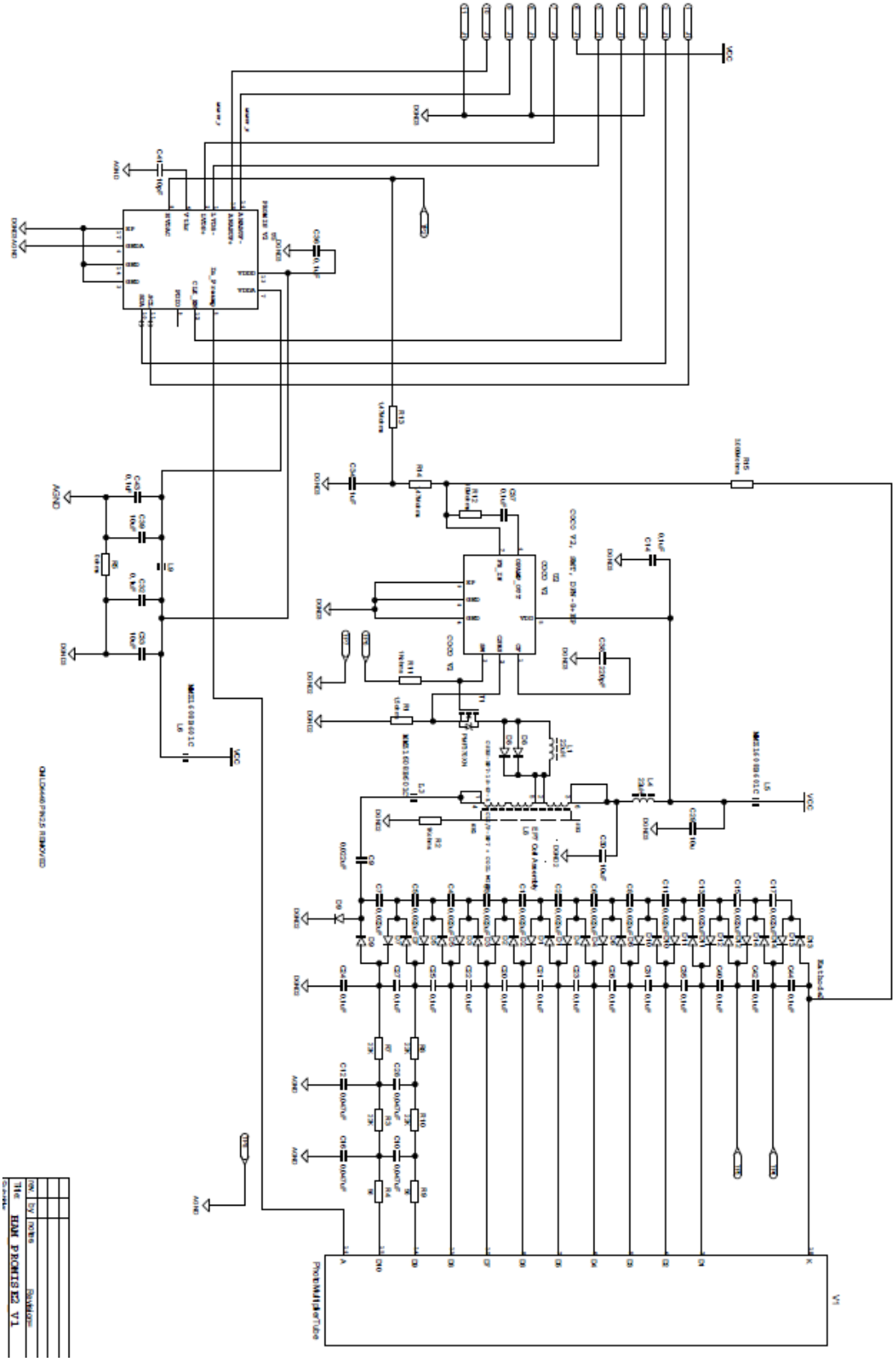
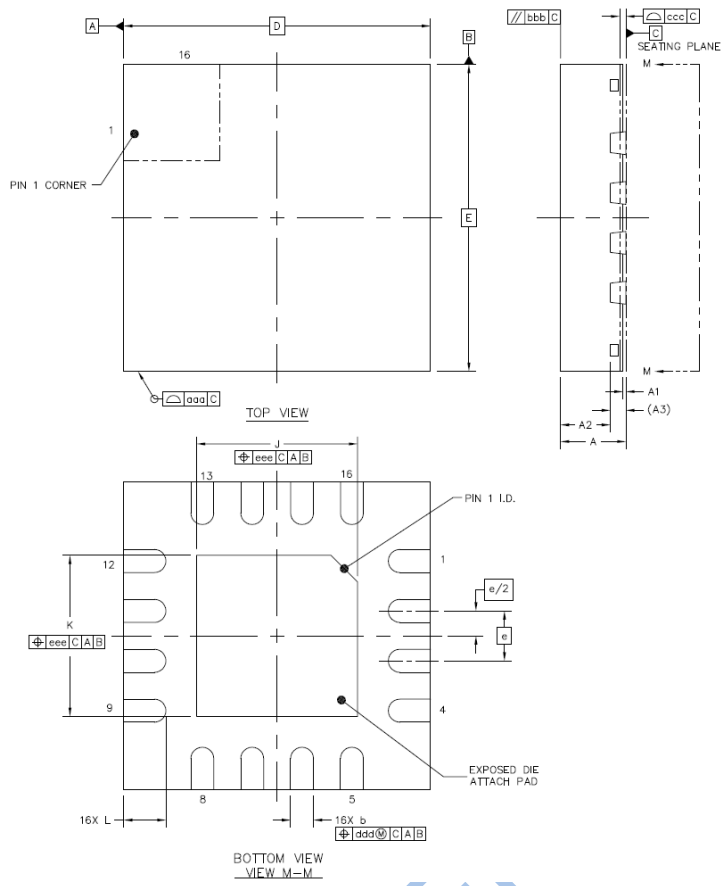


Figure 3 PMT Base schematic. PROMiS is used to read out a PMT.

Package Dimensions



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.25	0.3	0.35
BODY SIZE	X	D		4 BSC	
	Y	E		4 BSC	
LEAD PITCH		e		0.65 BSC	
EP SIZE	X	J	2	2.1	2.2
	Y	K	2	2.1	2.2
LEAD LENGTH		L	0.5	0.55	0.6
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

Figure 4 PROMiS available in QFN16 plastic package. All dimensions in mm.

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