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Lotto B: Capitolato Tecnico
Lotto B: Technical Specifications

CMS Silicon Pixel R&D for Phase II

Chapters:

0. Introduction
1. Batch-1 Device technical details
2. Batch-2 Device technical details
3. Single Chip assembly
4. Processing Schedule and Quality Assurance
5. Acceptance Criteria

RD

0. Introduction

The Compact Muon Solenoid (CMS), experiment at the Large Hadron Collider (LHC) at CERN, planned the upgrade of the silicon pixel detector for the Phase II. This upgrade intends to replace the current pixel tracker with a new high efficiency and low mass detector. The conceptual layout is under study and the goal of the R&D in this proposal is to design and qualify the best performing and radiation tolerant pixel detector for Phase II upgrade.

In this proposal we are going to discuss the production of two lots of pixel devices. First lot (***Batch-1***) foresees the production of fully functional single ROC chip devices, while second lot (***Batch-2***) plan the production of dummy devices designed to study the bump bonding technology for high density of bumps.

The deliverables for this bid will be thinned, diced and single-chip assembled units that pass the acceptance criteria, the test results, and the process details, all as specified in following chapters.

In the following:
1) **batch-1** or **batch-2** identify the name of lots to be assembled. Details will be discussed in the following pages.

2) **INFN-Pisa** identifies the laboratory in charge of this R&D proposal.

1. Batch-1: device technical details

1.1. Overview

This document contains the technical specification for the upgrade of the CMS pixel detector for Phase II and focuses on the silicon pixel device hybridization.

As non-exhaustive example we are showing here the basic unit of a prototypes to be produced by this R&D project. It consists of a readout chips (ROC) electrically connected by bump-bonds to a pixel silicon sensor. In the current prototype design each ROC has 52 columns × 80 rows and the unit size of a pixel sensor is 150μm × 100μm. The picture of the current pixel device is shown in Figure 1a with a few implant details shown in the Figure 1b. The project will deal also with different devices having larger number of columns and rows with modified pixel geometry and pitch.

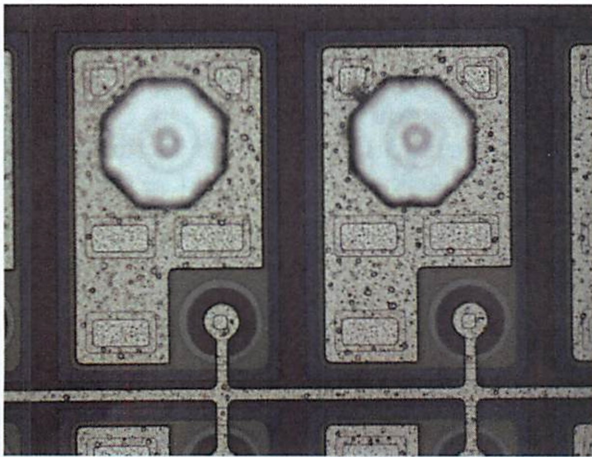

Figure 1a: Close view of 150μm x 100μm pixel

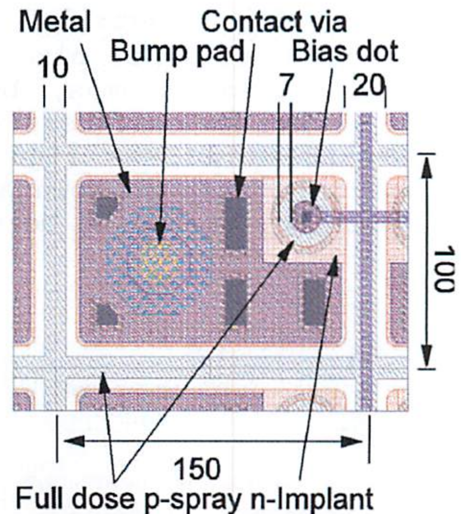

Figure 1b: Detail of the Pixel Unit Cell for a of 150μm x 100μm pixel. All distances are in μm.

The R&D discussed in this document plan to the optimization of the pixel unit design, following the qualification of new prototypes having the following main features:

- smaller pixel pitch, compared to current design;
- thinner active and full thickness, compared to standard of 300 μm in use;
- higher electrical interconnection density;
- improved radiation tolerance;

as specified in the following for **batch-1** and **batch-2** lots.

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1.2. Batch-1 Wafer description

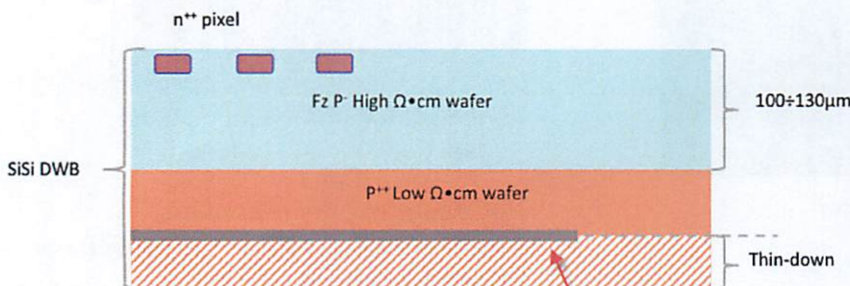
1.2.1. Pixel Sensor Wafer description

The pixel devices are fabricated with Single Sided process on 6-inch diameter wafers, silicon-silicon Direct Wafers Bonded (***DWB***) and SOI wafers, built on a low resistivity carrier wafer (p-type doped) as support of a high resistivity p-type FZ wafer as active layer in which the devices are processed. Support wafer is 500 μm thick while two active wafer layer thicknesses are available: 100 μm and 130 μm.

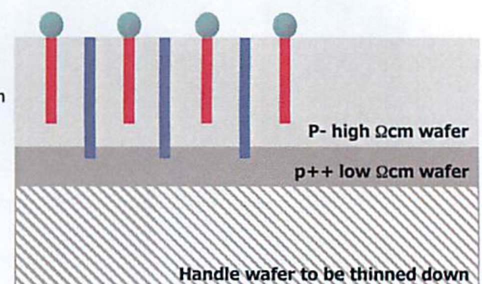
Wafers to be used in this project are processed with two different technologies:

- Planar pixels with junction build as layer on the surface by planar implant doping (design-A), see Figure 2a. This design will implement also Active/Slim edge as detailed in the next paragraph;
- 3D columnar pixel, having junction made by cylindrical doped columns, build by DRIE technology through the active thickness (***design-B***), see Figure 2b.

As shown in the figures handle wafer on the deliverables will be thinned down and eventually backside after thinning will be covered by metal contact layer.



2a: Design-A cross section of SiSi DWB wafer. Metal contact in the thinned backside is shown, sketch view not in scale



2b: Design-B cross section of SiSi DWB wafer. Columnar implantation are shown: red are n+ doped (Junction), blue column p+ doped (Ohmic). Sketch view not in scale.

For both Design-A and Design-B sensor wafers will pass a QA procedure prior delivery to the vendor for hybridization, and a Known Good Die (KGD) map will be provided together with the wafers.

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1.2.2. Design-A Layout details

Design-A wafer layout is shown in Figure 3.
The GDS file will be made available for mask design. Layout includes different pixel devices to be used in this project. Devices are grouped as underlined in the figure. The name is inherited by the corresponding ROC to be used in the hybridization process. For this project devices assembled with PSI type ROC chips will be used.
The devices naming convention and details for the pitch (units are in μm) are shown in the table 1.

PSI46dig	FCP130	RD53A	FE-I4	R4S	CLIC-PIX
			single & double	new PSI test roc	
100 x 150 std	30 x 100	50x50	50 x 250 std.	50x50	50x50
50 x 50 adapt.		25 x 100		25 x 100	
25 x 100 adapt.					

***Table 1**: Names and pixel pitch details (in μm) of devices implemented in Design-A*

In the table the specification "std." means standard devices with pixel pitch similar to ROC chip; "adapt." identify devices with smaller pixel pitch adapted to the larger ROC chip pitch.

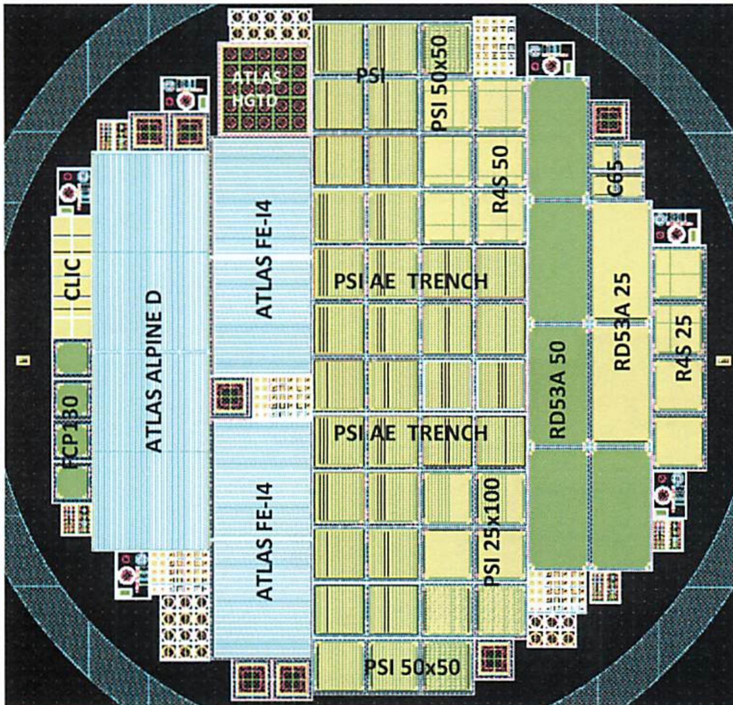

Figure 3: Layout of the Design-A wafer

In order to spot challenges for the hybridization steps a few layout details are listed in the following.

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Detail of a typical device in the periphery region is shown in Figure 4. It can be seen the corner of a device with dashed "staggered trench" and dicing lines. Cross section showing the geometry of a typical "trench" is shown in Figure 5: implant is built in depth through the active devices down to the carrier wafer. In order to exploit the performance of the trench design a second set of dicing lines are drawn, Optional dicing lines, designed nearby the trench structure (Figure 4).
In addition to the pixel devices the wafer includes, for the two layouts, test structures, diodes, gate-controlled diodes, MOS capacitors, and fiducial markers.

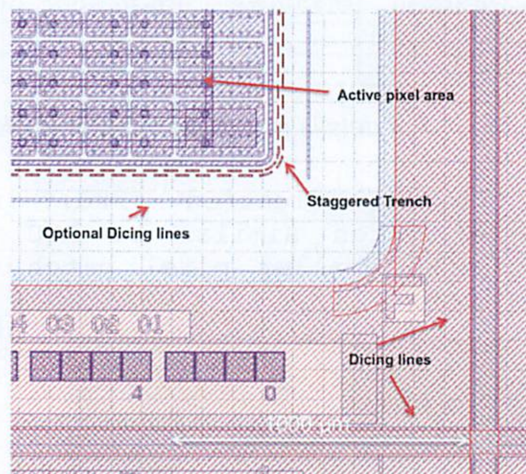

Figure 4: Corner of a Design-A device. Dicing Lines (path width 85 μm) and Trench implant can be seen.

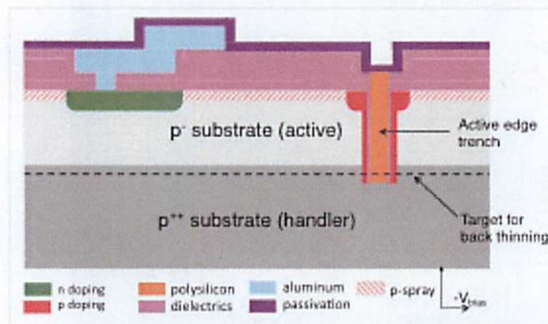

Figure 5: Cross section of a periphery trench implant, sketch view not in scale.

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1.1.1. Design-B Layout details

Design-B wafer layout is shown in Figure 6.
The GDS file will be made available for mask design. Layout includes pixel devices to be used in this project. Devices are grouped as underlined in the figure. The name is inherited by the corresponding ROC to be used in the hybridization process. For this project devices assembled with PSI type ROC chips will be used.
The devices naming convention and details for the pitch (units are in μm) are shown in the table 2.

FE-I4 (ATLAS)	FE-I3 (ATLAS)	PSI46dig (CMS)	FCP	RD53
50 x 250 (2E) std	50 x 50 (1E)	100 x 150 (2E and 3E) std.	30 x 100 (1E)	50x50 (1E)
50x50 (1E)	25 x 100 (1E and 2E)	50x50 (1Eand2E)		25 x 100 (1E)
25x100 (1Eand2E)		50x100,100x100 (2E+4E)		25 x 100 (2E)
25 x 500 (1E)		50x100,100X150 (2E+6E)		
		25 x 100 (1E and 2E)		

***Table 2**: Names and pixel pitch details (in μm) of devices implemented in Design-B*

In the table specification "1E or 2E etc." means devices processed with Pixel Unit CEL (*PUC*) made by 1 or more columnar cells. As before "std." means PUC with pitch similar to the corresponding ROC chip.

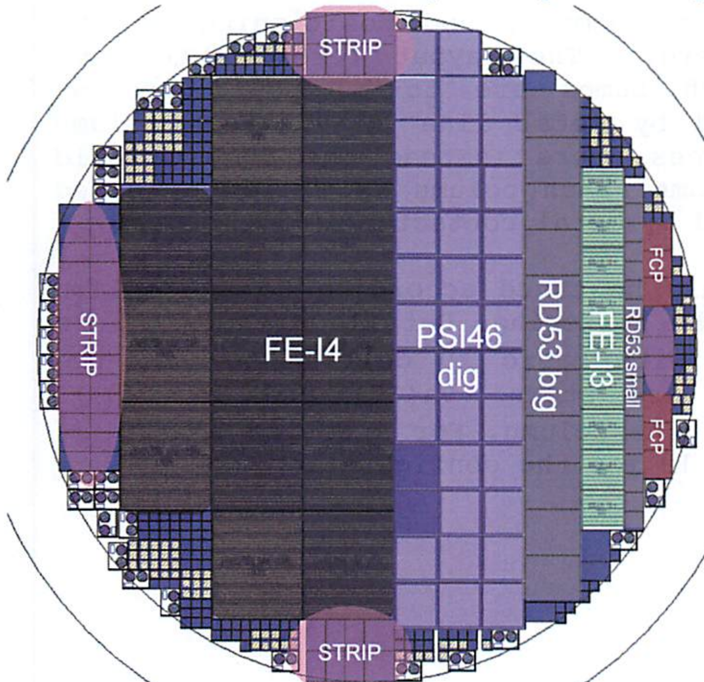

Figure 6: Design-B wafer Layout

In order to spot challenges for the hybridization steps a few layout details are listed in the following.

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Detail of a typical device in the periphery region is shown in Figure 7. It can be seen the corner of a 3D device with dicing lines, columnar periphery termination and the structure numbering.

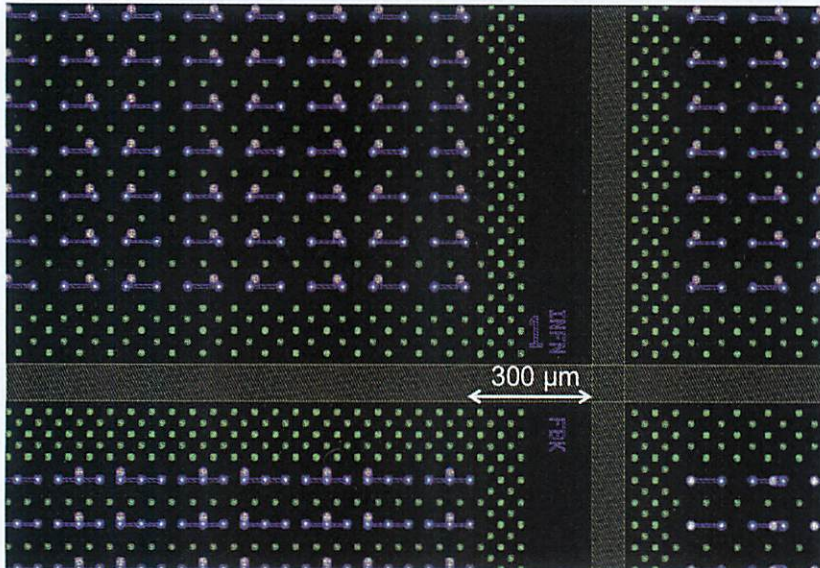

Figure 7: Corner of a 3D device (id n.1) included in Design-B. Dicing path width is 80 µm.

A few details on column geometry and positioning of the bumps are discussed here. The layout foresees to have pixel devices in which bumps are to be positioned on specific pads connected by metal line to junction column implant and pixel devices where instead the bumps should stay on top of the column. Each column is filled by doped poly-silicon and covered by metal contact.

The bump dimension should be tuned according to the column geometry discussed in the following. Details are visible in figure 9 for a device with basic 3D cell 50X50 μm^2, two different arrangements are shown (9a(1E) and 9b (2E)). Bumps are not on top of the column. For a device 25X100 μm^2 cell is shown in figure 10 for the configuration 2E.

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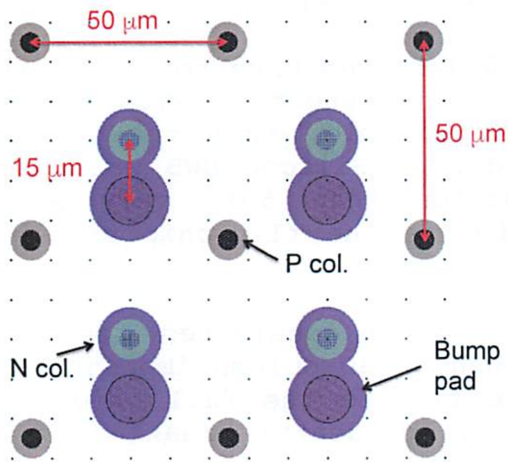

Figure 9a: *3D cell for a device 50 μm x 50 μm*

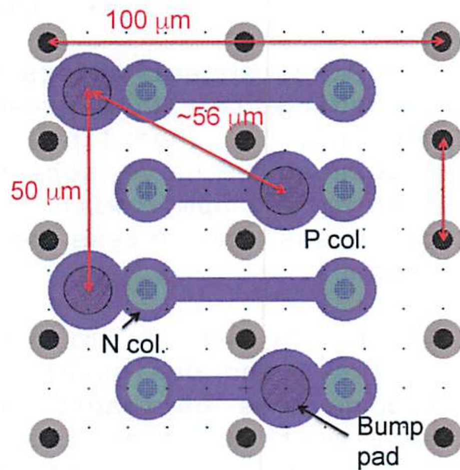

Figure 9b: *3D cell for a device 50 μm x 50 μm*

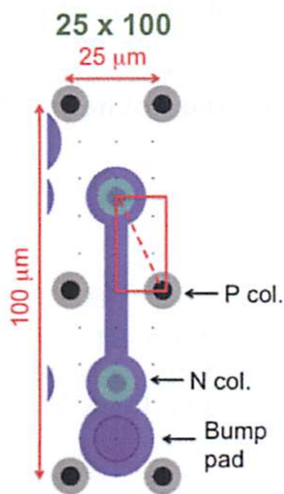

Figure 10: 3D cell for a device 25 μm x 100 μm

In addition to the pixel devices the wafer contains, for the two layouts, test structures, diodes, gate-controlled diodes, MOS capacitors, and fiducial markers.

1.2. Pixel Wafer thinning for Batch-1

The Pixel sensor wafers thick 600-630 μm have to be thinned according to INFN prescription and under agreement with company. We underline here, as example, that the smaller thickness we have achieved today on Silicon DWB wafers is 180 μm ± 5μm, with TTV smaller than 5μm, very small roughness and stress release before the flip-chip assembly process.

Tuning of wafer thinning has to be considered for both design-A and design-B; the trench or 3D column implant near the devices periphery can make fragile the full wafer and this must be taken into account. Accidental breaking of no more than one wafer it is an acceptable risk.

The vendor has to take precautions, ESD and mechanical, in order to protect the wafer, the PUC and UBM from any damage during the thinning process: the wafers have to be suitably protected against any damage to the wafer (chipping, cracking, or shattering) and on bumps and other exposed metal layer structures.

1.3. ROC Wafer Description

Batch-1 devices (both design–A and design–B) will be connected with bump bonding to the readout chips (ROC) processed in 8-inch in diameter and with standard thickness (750–825 μm).

Each readout chip is processed by standard CMOS technology: 0.25 μm technology for PSI46dig and PROC600.

Each ROC PSI46dig measures about 10.2 mm x 7.9 mm. There are 62 four-ROCs blocks ("reticle") on each wafer as shown in Figure 11 for a total of 248 chips, with 100 μm X 150 μm pitch. Similar layout and geometrical features are valid for the other PSI ROC wafer to be used in this project PROC600.

For PROC600 each reticle hosts 3 ROC chips equivalent to PSI46dig plus one ROC4sens with pitch 50 μm in both directions.

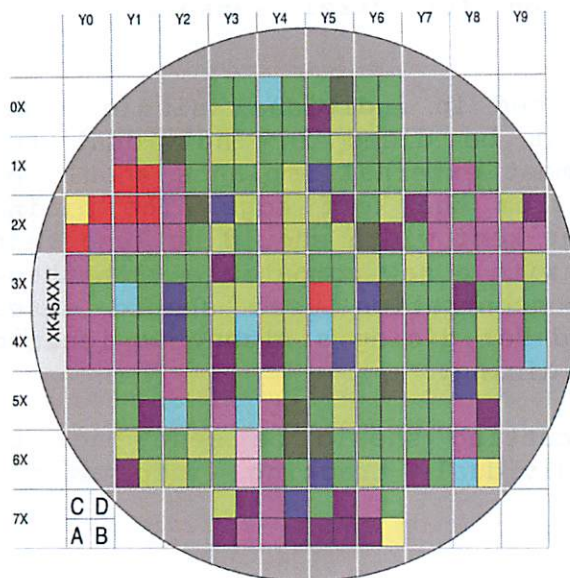

Figure 11: Floor plan of PSI46dig ROC wafer. ROCs are organized in blocks of four chips (according to lithography reticle), 248 in total.

The chips will be tested on the wafer before the delivery to hybridization vendor and a Known Good Die (KGD) map will be provided together with the wafers.

1.3.1. ROC Wafer thinning

The ROC wafers, PSI46dig and PROC600, have to be thinned to a standard thickness usually around 175μm ± 5μm, with TTV smaller than 5μm, very small roughness and stress release before the flip-chip assembly process.
The vendor has to take precautions, ESD and mechanical, to protect the wafer and the bumps from any damage during the thinning process. The wafers have to be suitably protected against any damage to the wafer (chipping, cracking, or shattering), the bumps, and the wire bond pads.

All wafer remnants after cutting should be sent back to INFN-Pisa with their individual tracking information, including wafer number.

1.4. Dicing specification for Pixel sensors devices and ROC chip

The pixel wafers must be diced in individual single Pixel sensors and ROC wafers must be diced in individual ROC chips. All guard rings or most external implants should be at least 30 microns away from the kerf edge. The dicing tolerance is ±20 microns. The kerf width should be less than 50μm. Dicing should be done with a saw compatible with these specifications. The grit/concentration used should agree with the industrial standard for dicing silicon. De-ionized water should be used during dicing.

All wafer remnants after cutting should be sent back to INFN-Pisa with their individual tracking information, including wafer number.

2. Batch-2: device technical details

2.1. Overview

The goal of this processing is the study of Bump Bonding with high interconnection density. Today we have experience with prototypes assembled with about 5000 bumps/cm^2. Future pixel detectors will be hybridized with an interconnection density ~6-10 times higher. Realistic design for such detectors foresees a unit sensitive area of ~4 cm^2, and the detector unit is built by hybridization of one ROC and one pixel sensor.

For this study we plan to use pixel devices and ROC not fully functional as detectors (dummy devices), built by metal layer deposition on virgin silicon wafers. In order the test consistently the bump bonding process at vendor the plan foresees the use of 8-inch or 6-inch wafers for ROC and 6-inch wafer for sensor dummy devices.

The silicon material has to be thinned and diced (for specification see details described for batch-1) in order to evaluate the final assembly performance after the full processing steps and in standard conditions.

2.2. Batch-2 Wafer description

2.2.1. Pixel Sensor and ROC Wafer description

The basic functionalities to be studied with a target detector unit of ~4 cm^2 area and thinned thickness, are the following:

- Count of bump defects for unit detector
- Measurement of interconnection resistance of bumps, with 4 points method.

The proposal consists of a design of a set of test structures build by arrays of bump bonds, in which an optimized fraction of them have been connected, in one direction, by metal lines to form daisy chains, and the rest are short-circuited, in the same direction, to connect the daisy chains to the external pad connections.

The test structure is actually a whole assembly, and therefore, composed of two sides for the flip chip process. One of them is the 'chip' side ("Dummy ROC" c-side processed on 8 inch wafer or 6 inch wafer) with the metal pattern to make one half of the daisy chains, plus the corresponding fan-out to the test pads for automatic testing. The 'detector' side ("Dummy Sensors" d-side processed on 8 inch wafer or on 6 inch wafer) contains only the corresponding metal pattern to match with the c-side forming the daisy chain structure. Wafer size selection is left to vendor choice.
The daisy chains are uniformly distributed in the test structure in order to cover the whole assembly area of about 4 cm^2.
In addition, two ground busses, with all their bump bonds short-circuited, cross the assembly in perpendicular directions roughly at the middle of the assembly in order to facilitate the connection of the daisy chains to ground for the testing.
The test structure is therefore, a full assembly made of a series of long bump bond daisy chains that are evenly distributed across the whole area of the assembly.
Each daisy chain contains a number N of bump bonds tuned considering the quality test significance. Each chain is connected in a way that if any of them fails, the whole chain is electrically open. Figure 12 shows a schematic cross-section of a daisy chain in the assembly.

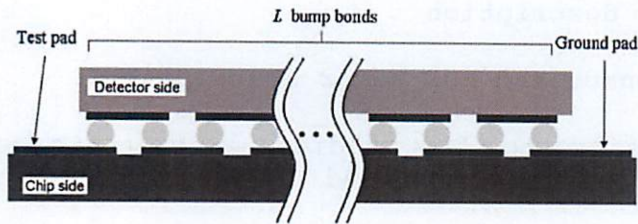

Figure 12: cross section of a device implemented in Batch-2 Layout

The chains are then connected to test pads prepared for automated measurements with a probe station.

The layout will be discussed between vendor and INFN-Pisa: INFN-Pisa will provide basic cell design (drawing) for connections that will be modified and implemented by the vendor in a gds file for masks preparation.

This study should consider, for a "typical future detector", a density of 160000-320000 (50μ x 50μ - 100μ x 25μ pitch) bumps on a 4 cm^2 device.
The goal consists in verifying the feasibility of the hybridization step for a "typical future detector".
In order to face realistic processing issues we target also on thinning dummy pixel wafer and dummy ROC wafer down to about 200 μm. The actual limit will be discussed with the vendor.

As comparison it is foreseen the design of standard devices with bumps density as commonly used today too.
The wafers layout will be discussed and agreed between INFN-Pisa and vendor.

Vendor should be capable to provide the full process:

- GDS layout design
- Mask preparation
- Wafer procurement
- Metal layer deposition steps
- Oxidization step and opening on passivation
- Any extra layer deposition deemed necessary by the vendor for the bump bonding technology selected and agreed with INFN-Pisa
- All steps as discussed previously for hybridization of batch-1

The number of wafers processed is planned to be small: for "ROC dummy" wafers 1-2 ROC 8-inch wafers or 2-3 6-inch wafers, for "Sensor dummy" 2-3 6-inch or 8-inch wafers.

20

Bump geometry details will be discussed and agreed with INFN-Pisa in order to maximize yield and performance.

3. Single Chip assembly

3.1. General consideration on Single Chip Assembly Procedure

The assembly of the modules has the following steps:

1) Production of the masks for Bumps and UBM deposition according to the GDS files provided for batch-1 by INFN-Pisa, provided by the vendor for batch-2. This is done preliminary to the production.
2) Bump deposition and/or UBM deposition on ROC and or on Pixel sensor wafers.
   The bump center-to-center spacing is from 100 μm down to 50 μm for batch-1, 50 μm for batch-2, in the smallest dimension. The bump pattern is replicated in columns and rows on each of the ROCs and matches the same pattern on the pixel sensor.
3) Photoresist protection of the bumps, that has to be done before thinning and dicing.
4) Thinning of the ROC and sensor wafers as specified above. Thinning must include grinding defect removal and surface polishing.
5) Dicing/cutting of the ROC wafers and Pixel sensor wafers.
6) Test of the basic ROC functionality after thinning and dicing on tape. The feasibility and the procedure of this test will be discussed and agreed between vendor and INFN-Pisa.
7) Flip-chip assembly of the ROCs to pixel sensor.
8) Visual inspection and recording of inspection data at each step.
9) Each ROC after Flip Chip Bump Bonding should be X-ray inspected and recorded picture should be made available.
10) Prototypes delivery should be done with appropriate packaging (ESD safe). The packaging should be discussed with INFN-Pisa prior to shipment.

Other tests to be specified by the vendor and agreed upon by INFN-Pisa can also be performed for QA purposes.

The vendor should provide data in electronic/numeric format: in order to reveal the bump, interconnection or wafer characteristics, pairing of ROCs on Large Pixel sensors, possible ROC reworking, etc. The vendor should

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inform INFN-Pisa about possible technical problems or any other delays as early as possible.

3.1.1. Bump deposition and Flip-Chip specifications

The primary requirement for deposition of bumps (and/or UBM) on the sensor and ROC wafers is to meet the fine-pitch specification with high yield, which will allow the subsequent flip-chip assembly of the chips to the sensor with high yield of low electrical resistance connections. Details listed in the following refers to hybridization of Batch-1, specific chapter is dedicated to Batch-2.

Specific requirements are:

1) Bump material composition must be specified by the vendor and approved by INFN-Pisa. Same process for UBM, used to match the bump material and to provide high yield during flip-chip assembly, long-term high quality contacts and avoid migration of Bump material inside the wafer.
2) The process temperature profile must be specified with a maximum of 350 °C.
3) Flux less process should be used.
4) Center to center Bump pitch: 50 μm minimum.
5) The bump diameter should be not larger than 40 μm, for PROC600 to be optimized according to layout constraints.
6) Passivation opening for bump: according to point 5).
7) Alignment accuracy of flip-chip process: better than 3 μm
8) Bump height after flip-chip assembly: minimum 15 μm
9) Bump Uniformity: $\leq$ 2 μm (wafer 8″)
10) Electrostatic discharge protection required during wafer handling and flip-chip assembly.
11) Additional processing on the bare module (wire bonding, gluing and component mounting) will be necessary after the hybridization. The bump deposition and flip-chip processing must be compatible with these additional assembly steps.
12) The wire bonding pads should be left clean by the process to ensure an easy and safe wire bonding with automatic equipment. Wire bonding tests, on sample, will be made on test structures from the ROC wafers before and after bumping to verify that the pads have not been degraded during the processing.

RD

The following points constitute additional criteria for deliverables acceptance; reference values are listed in Chapter 3 (**Acceptance Criteria**):

13) Missing or merged bump defect rate, as determined by visual inspection on a wafer, and after flip-chip assembly as determined by X-ray inspection or other means should smaller than 2% per device unit.
14) The chips should adhere firmly to the sensor after mating, and should detach only if pull force larger than 0.2 g/bump (Indium bump material) or 1.5 g/bump (other bump materials).
15) The total leakage current of a sensor must not increase too much after the dicing process. In particular the device should be operational at least up to the depletion voltage before the hybridization step.

3.1.2. Single Chip Assembly High density Bump Bonding project

The single chip assembly for Batch-2 follows similar specification listed previously for Batch-1 with the exception of following points: 4), 5), 6), 8) and 15).
Bump and UBM geometry (points 4), 5), 6) and 8)) should be optimized according to the device pitch.
The point 15) is not applicable given that we are using dummy devices.

After approval of the vendor wafer Layout the proposal for bump, UBM geometry and material will be discussed and agreed with INFN-Pisa.

3.2. Materials provided

3.2.1. By CMS

For the Batch-1 production run, INFN-Pisa will provide to the vendor:

1) Up to 6 pixel silicon sensor wafers (DWB or SOI, 150 mm diameter).
2) Up to two silicon ROC wafers (200 mm diameter).
3) Files of the wafers layout in GDS format.
4) Conceptual drawing of Benzo-Cyclo-Butene (BCB) mask.
5) KGD map for each ROC wafers and KGD map showing the good pixel sensors on the sensor wafers based on our

tests. Only the good ROC dies and pixel sensors should be used in the assembly process.

For the Batch-2 production run, INFN-Pisa will provide to the vendor:

1) Conceptual sketch agreed with the vendor, of ROC and Sensor wafer Layout

3.2.2. By Vendor

For the Batch-2 production run, the vendor will provide
1) Dummy Pixel silicon sensor wafers,(6-inch or 8-inch).
2) Dummy silicon ROC wafers (6-inch or 8-inch).
3) Files of the wafers layout in GDS format.
4) KGD dies map after optical inspection of parts.

3.3. Materials to be processed in this project

Vendor bid should be issued accordingly to the following list:

3.3.1. Batch-1 Design-A and B

Pixel wafers:
1. Units to be processed: 2 Design-A + 2 Design-B. Appropriate mask should be designed and produced.
2. Back side metallization: a uniform metal layer should be sputtered in the backside after wafer thinning. No masking is required unless this is deemed necessary by the vendor.
3. Exclusively for Design-A: a Benzo-Cyclo-Butene (BCB) protection layer should be deposited on the wafer in order to protect devices from sparks. Appropriate mask should be designed and produced.

Quotation should detail the cost for "first wafer" processed for both designs, for the "second wafers" (and for eventual more wafers beyond this offer).

ROC wafers:

4. Units to be processed: one PROC600 wafer. Appropriate mask should be designed and produced
5. BCB protection layer should be deposited on the PROC600 wafer in order to protect devices from sparks. Appropriate mask should be designed and produced.

Quotation should detail the cost for "first wafer" processed (and for eventual more wafers beyond this offer).

Flip Chip Bump bonding:

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CMS Silicon Pixel R&D for Phase II

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RD

0. Introduction

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In the following:
1) **batch-1** or **batch-2** identify the name of lots to be assembled. Details will be discussed in the following pages.

2) **INFN-Pisa** identifies the laboratory in charge of this R&D proposal.

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1. Batch-1: device technical details

1.1. Overview

This document contains the technical specification for the upgrade of the CMS pixel detector for Phase II and focuses on the silicon pixel device hybridization.

As non-exhaustive example we are showing here the basic unit of a prototypes to be produced by this R&D project. It consists of a readout chips (ROC) electrically connected by bump-bonds to a pixel silicon sensor. In the current prototype design each ROC has 52 columns × 80 rows and the unit size of a pixel sensor is 150μm × 100μm. The picture of the current pixel device is shown in Figure 1a with a few implant details shown in the Figure 1b. The project will deal also with different devices having larger number of columns and rows with modified pixel geometry and pitch.

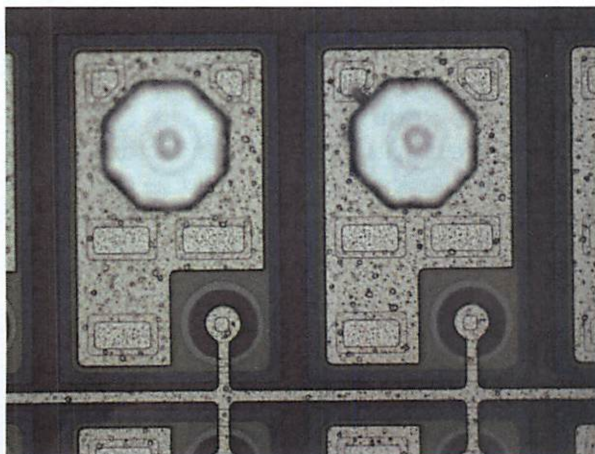

Figure 1a: Close view of 150μm x 100μm pixel

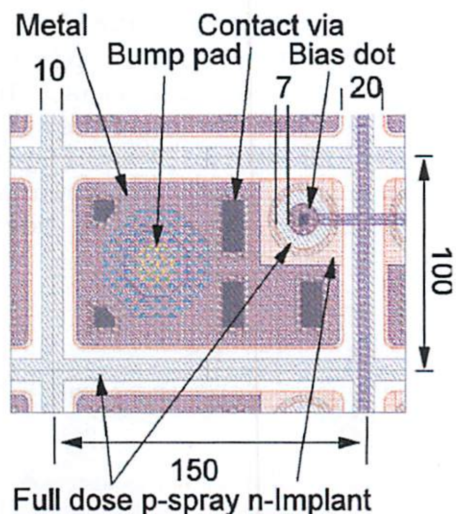

Figure 1b: Detail of the Pixel Unit Cell for a of 150μm x 100μm pixel. All distances are in μm.

The R&D discussed in this document plan to the optimization of the pixel unit design, following the qualification of new prototypes having the following main features:

- smaller pixel pitch, compared to current design;
- thinner active and full thickness, compared to standard of 300 μm in use;
- higher electrical interconnection density;
- improved radiation tolerance;

as specified in the following for **batch-1** and **batch-2** lots.

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1.2. Batch-1 Wafer description

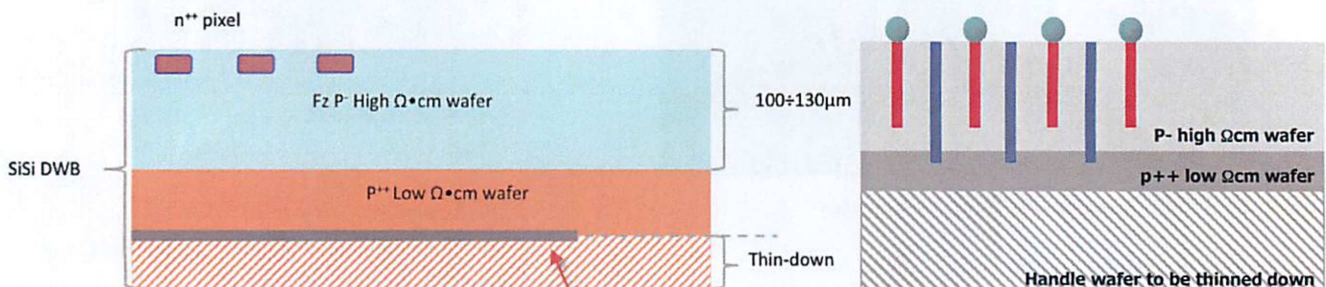
1.2.1. Pixel Sensor Wafer description

The pixel devices are fabricated with Single Sided process on 6-inch diameter wafers, silicon-silicon Direct Wafers Bonded (***DWB***) and SOI wafers, built on a low resistivity carrier wafer (p-type doped) as support of a high resistivity p-type FZ wafer as active layer in which the devices are processed. Support wafer is 500 µm thick while two active wafer layer thicknesses are available: 100 µm and 130 µm.

Wafers to be used in this project are processed with two different technologies:

- Planar pixels with junction build as layer on the surface by planar implant doping (design-A), see Figure 2a. This design will implement also Active/Slim edge as detailed in the next paragraph;
- 3D columnar pixel, having junction made by cylindrical doped columns, build by DRIE technology through the active thickness (***design-B***), see Figure 2b.

As shown in the figures handle wafer on the deliverables will be thinned down and eventually backside after thinning will be covered by metal contact layer.



2a: Design-A cross section of SiSi DWB wafer. Metal contact in the thinned backside is shown, sketch view not in scale

2b: Design-B cross section of SiSi DWB wafer. Columnar implantation are shown: red are n+ doped (Junction), blue column p+ doped (Ohmic). Sketch view not in scale.

For both Design-A and Design-B sensor wafers will pass a QA procedure prior delivery to the vendor for hybridization, and a Known Good Die (KGD) map will be provided together with the wafers.

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1.2.2. Design-A Layout details

Design-A wafer layout is shown in Figure 3.
The GDS file will be made available for mask design. Layout includes different pixel devices to be used in this project. Devices are grouped as underlined in the figure. The name is inherited by the corresponding ROC to be used in the hybridization process. For this project devices assembled with PSI type ROC chips will be used.
The devices naming convention and details for the pitch (units are in μm) are shown in the table 1.

PSI46dig	FCP130	RD53A	FE-I4	R4S	CLIC-PIX
			single & double	new PSI test roc	
100 x 150 std	30 x 100	50x50	50 x 250 std.	50x50	50x50
50 x 50 adapt.		25 x 100		25 x 100	
25 x 100 adapt.					

***Table 1**: Names and pixel pitch details (in μm) of devices implemented in Design-A*

In the table the specification "std." means standard devices with pixel pitch similar to ROC chip; "adapt." identify devices with smaller pixel pitch adapted to the larger ROC chip pitch.

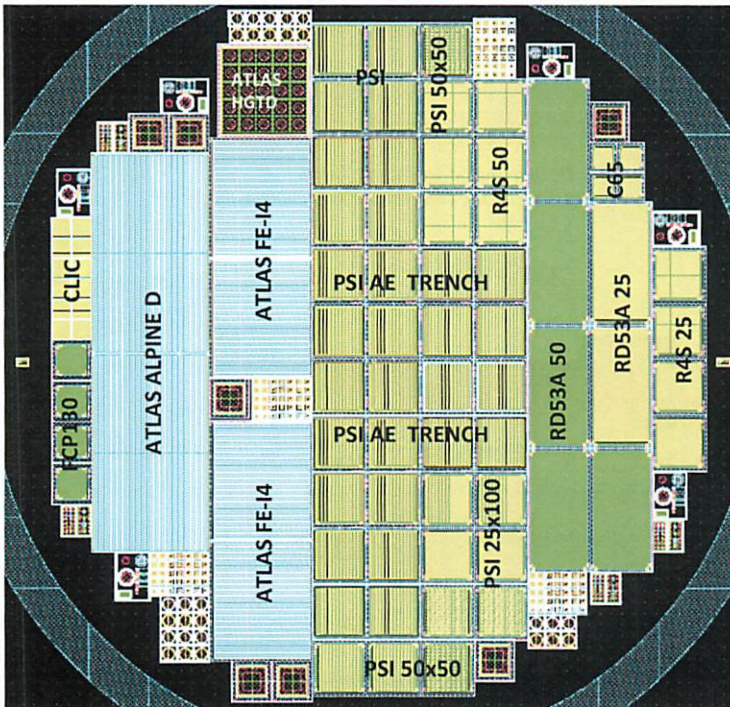

Figure 3: Layout of the Design-A wafer

In order to spot challenges for the hybridization steps a few layout details are listed in the following.

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Detail of a typical device in the periphery region is shown in Figure 4. It can be seen the corner of a device with dashed "staggered trench" and dicing lines. Cross section showing the geometry of a typical "trench" is shown in Figure 5: implant is built in depth through the active devices down to the carrier wafer. In order to exploit the performance of the trench design a second set of dicing lines are drawn, Optional dicing lines, designed nearby the trench structure (Figure 4).
In addition to the pixel devices the wafer includes, for the two layouts, test structures, diodes, gate-controlled diodes, MOS capacitors, and fiducial markers.

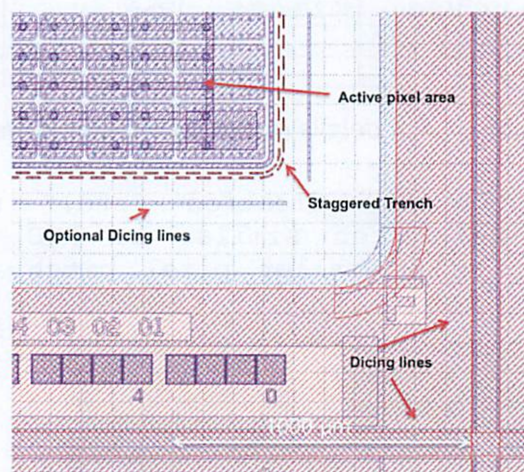

Figure 4: Corner of a Design-A device. Dicing Lines (path width 85 μm) and Trench implant can be seen.

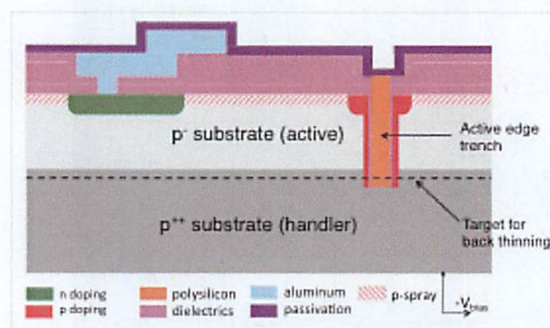

Figure 5: Cross section of a periphery trench implant, sketch view not in scale.

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1.1.1. Design-B Layout details

Design-B wafer layout is shown in Figure 6.
The GDS file will be made available for mask design. Layout includes pixel devices to be used in this project. Devices are grouped as underlined in the figure. The name is inherited by the corresponding ROC to be used in the hybridization process. For this project devices assembled with PSI type ROC chips will be used.
The devices naming convention and details for the pitch (units are in μm) are shown in the table 2.

FE-I4 (ATLAS)	FE-I3 (ATLAS)	PSI46dig (CMS)	FCP	RD53
50 x 250 (2E) std	50 x 50 (1E)	100 x 150 (2E and 3E) std.	30 x 100 (1E)	50x50 (1E)
50x50 (1E)	25 x 100 (1E and 2E)	50x50 (1Eand2E)		25 x 100 (1E)
25x100 (1Eand2E)		50x100,100x100 (2E+4E)		25 x 100 (2E)
25 x 500 (1E)		50x100,100X150 (2E+6E)		
		25 x 100 (1E and 2E)		

***Table 2**: Names and pixel pitch details (in μm) of devices implemented in Design-B*

In the table specification "1E or 2E etc." means devices processed with Pixel Unit CEL (*PUC*) made by 1 or more columnar cells. As before "std." means PUC with pitch similar to the corresponding ROC chip.

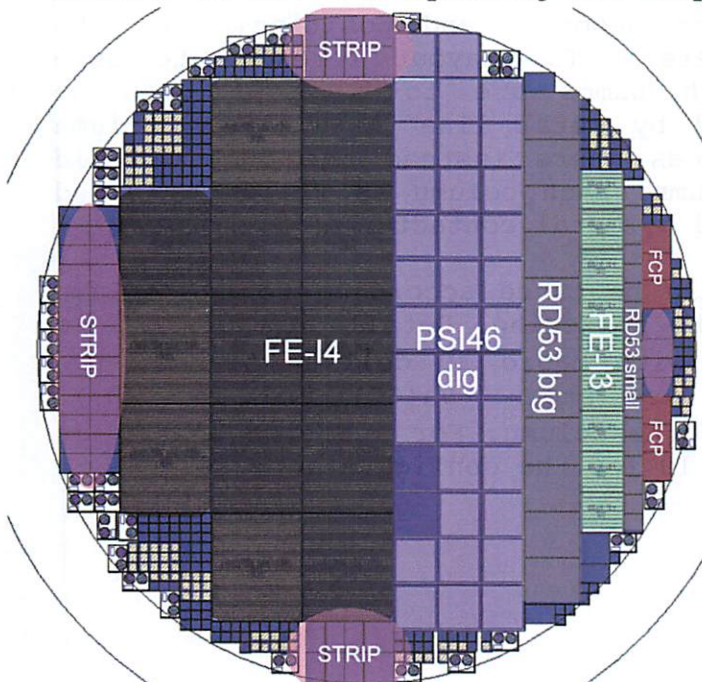

Figure 6: Design-B wafer Layout

In order to spot challenges for the hybridization steps a few layout details are listed in the following.

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Detail of a typical device in the periphery region is shown in Figure 7. It can be seen the corner of a 3D device with dicing lines, columnar periphery termination and the structure numbering.

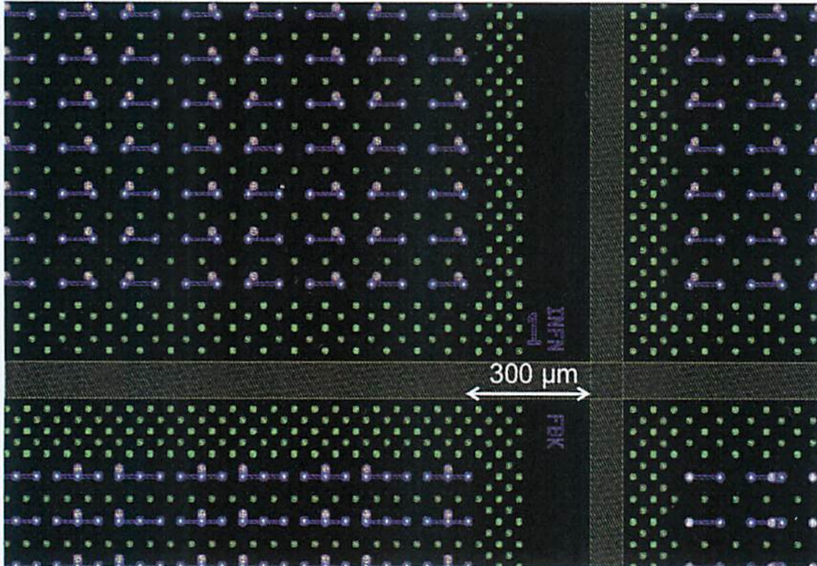

Figure 7: Corner of a 3D device (id n.1) included in Design-B. Dicing path width is 80 μm.

A few details on column geometry and positioning of the bumps are discussed here. The layout foresees to have pixel devices in which bumps are to be positioned on specific pads connected by metal line to junction column implant and pixel devices where instead the bumps should stay on top of the column. Each column is filled by doped poly-silicon and covered by metal contact.

The bump dimension should be tuned according to the column geometry discussed in the following. Details are visible in figure 9 for a device with basic 3D cell 50X50 μm^2, two different arrangements are shown (9a(1E) and 9b (2E)). Bumps are not on top of the column. For a device 25X100 μm^2 cell is shown in figure 10 for the configuration 2E.

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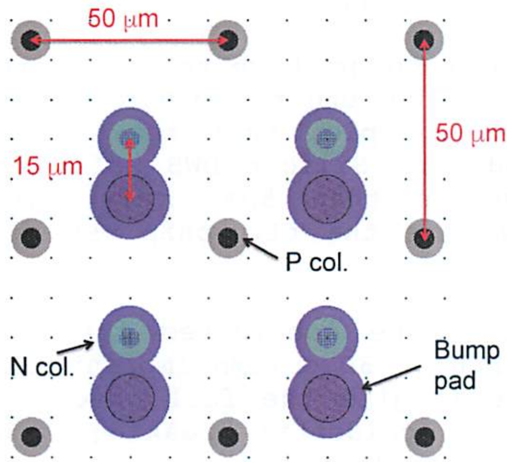

Figure 9a: *3D cell for a device 50 µm x 50 µm*

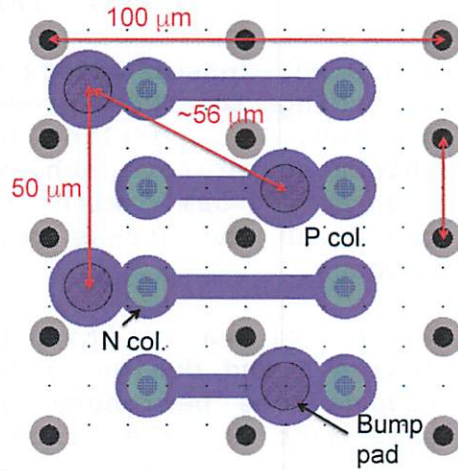

Figure 9b: *3D cell for a device 50 µm x 50 µm*

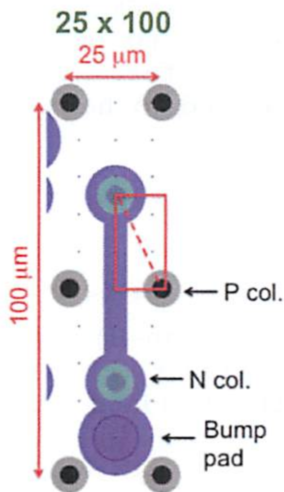

Figure 10: 3D cell for a device 25 µm x 100 µm

In addition to the pixel devices the wafer contains, for the two layouts, test structures, diodes, gate-controlled diodes, MOS capacitors, and fiducial markers.

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1.2. Pixel Wafer thinning for Batch-1

The Pixel sensor wafers thick 600-630 μm have to be thinned according to INFN prescription and under agreement with company. We underline here, as example, that the smaller thickness we have achieved today on Silicon DWB wafers is 180 μm ± 5μm, with TTV smaller than 5μm, very small roughness and stress release before the flip-chip assembly process.

Tuning of wafer thinning has to be considered for both design-A and design-B; the trench or 3D column implant near the devices periphery can make fragile the full wafer and this must be taken into account. Accidental breaking of no more than one wafer it is an acceptable risk.

The vendor has to take precautions, ESD and mechanical, in order to protect the wafer, the PUC and UBM from any damage during the thinning process: the wafers have to be suitably protected against any damage to the wafer (chipping, cracking, or shattering) and on bumps and other exposed metal layer structures.

1.3. ROC Wafer Description

Batch-1 devices (both design–A and design–B) will be connected with bump bonding to the readout chips (ROC) processed in 8-inch in diameter and with standard thickness (750–825 μm).

Each readout chip is processed by standard CMOS technology: 0.25 μm technology for PSI46dig and PROC600.

Each ROC PSI46dig measures about 10.2 mm x 7.9 mm. There are 62 four-ROCs blocks ("reticle") on each wafer as shown in Figure 11 for a total of 248 chips, with 100 μm X 150 μm pitch. Similar layout and geometrical features are valid for the other PSI ROC wafer to be used in this project PROC600.

For PROC600 each reticle hosts 3 ROC chips equivalent to PSI46dig plus one ROC4sens with pitch 50 μm in both directions.

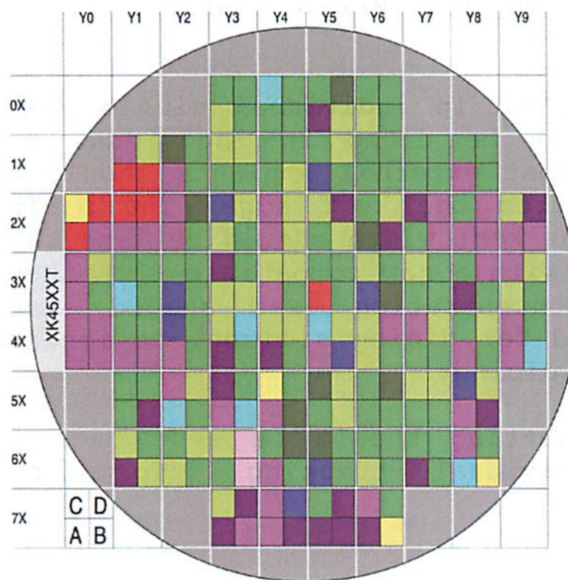

Figure 11: Floor plan of PSI46dig ROC wafer. ROCs are organized in blocks of four chips (according to lithography reticle), 248 in total.

The chips will be tested on the wafer before the delivery to hybridization vendor and a Known Good Die (KGD) map will be provided together with the wafers.

1.3.1. ROC Wafer thinning

The ROC wafers, PSI46dig and PROC600, have to be thinned to a standard thickness usually around 175μm ± 5μm, with TTV smaller than 5μm, very small roughness and stress release before the flip-chip assembly process.
The vendor has to take precautions, ESD and mechanical, to protect the wafer and the bumps from any damage during the thinning process. The wafers have to be suitably protected against any damage to the wafer (chipping, cracking, or shattering), the bumps, and the wire bond pads.

All wafer remnants after cutting should be sent back to INFN-Pisa with their individual tracking information, including wafer number.

1.4. Dicing specification for Pixel sensors devices and ROC chip

The pixel wafers must be diced in individual single Pixel sensors and ROC wafers must be diced in individual ROC chips. All guard rings or most external implants should be at least 30 microns away from the kerf edge. The dicing tolerance is ±20 microns. The kerf width should be less than 50μm. Dicing should be done with a saw compatible with these specifications. The grit/concentration used should agree with the industrial standard for dicing silicon. De-ionized water should be used during dicing.

All wafer remnants after cutting should be sent back to INFN-Pisa with their individual tracking information, including wafer number.

2. Batch-2: device technical details

2.1. Overview

The goal of this processing is the study of Bump Bonding with high interconnection density. Today we have experience with prototypes assembled with about 5000 bumps/cm^2. Future pixel detectors will be hybridized with an interconnection density ~6-10 times higher. Realistic design for such detectors foresees a unit sensitive area of ~4 cm^2, and the detector unit is built by hybridization of one ROC and one pixel sensor.

For this study we plan to use pixel devices and ROC not fully functional as detectors (dummy devices), built by metal layer deposition on virgin silicon wafers. In order the test consistently the bump bonding process at vendor the plan foresees the use of 8-inch or 6-inch wafers for ROC and 6-inch wafer for sensor dummy devices.

The silicon material has to be thinned and diced (for specification see details described for batch-1) in order to evaluate the final assembly performance after the full processing steps and in standard conditions.

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2.2. Batch-2 Wafer description

2.2.1. Pixel Sensor and ROC Wafer description

The basic functionalities to be studied with a target detector unit of ~4 cm^2 area and thinned thickness, are the following:

- Count of bump defects for unit detector
- Measurement of interconnection resistance of bumps, with 4 points method.

The proposal consists of a design of a set of test structures build by arrays of bump bonds, in which an optimized fraction of them have been connected, in one direction, by metal lines to form daisy chains, and the rest are short-circuited, in the same direction, to connect the daisy chains to the external pad connections.

The test structure is actually a whole assembly, and therefore, composed of two sides for the flip chip process. One of them is the 'chip' side ("Dummy ROC" c-side processed on 8 inch wafer or 6 inch wafer) with the metal pattern to make one half of the daisy chains, plus the corresponding fan-out to the test pads for automatic testing. The 'detector' side ("Dummy Sensors" d-side processed on 8 inch wafer or on 6 inch wafer) contains only the corresponding metal pattern to match with the c-side forming the daisy chain structure. Wafer size selection is left to vendor choice.
The daisy chains are uniformly distributed in the test structure in order to cover the whole assembly area of about 4 cm^2.
In addition, two ground busses, with all their bump bonds short-circuited, cross the assembly in perpendicular directions roughly at the middle of the assembly in order to facilitate the connection of the daisy chains to ground for the testing.
The test structure is therefore, a full assembly made of a series of long bump bond daisy chains that are evenly distributed across the whole area of the assembly.
Each daisy chain contains a number N of bump bonds tuned considering the quality test significance. Each chain is connected in a way that if any of them fails, the whole chain is electrically open. Figure 12 shows a schematic cross-section of a daisy chain in the assembly.

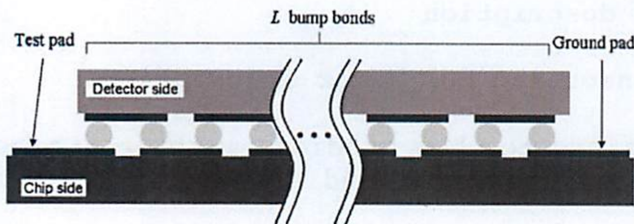

Figure 12: cross section of a device implemented in Batch-2 Layout

The chains are then connected to test pads prepared for automated measurements with a probe station.

The layout will be discussed between vendor and INFN-Pisa: INFN-Pisa will provide basic cell design (drawing) for connections that will be modified and implemented by the vendor in a gds file for masks preparation.

This study should consider, for a "typical future detector", a density of 160000-320000 (50μ x 50μ - 100μ x 25μ pitch) bumps on a 4 cm^2 device.
The goal consists in verifying the feasibility of the hybridization step for a "typical future detector".
In order to face realistic processing issues we target also on thinning dummy pixel wafer and dummy ROC wafer down to about 200 μm. The actual limit will be discussed with the vendor.

As comparison it is foreseen the design of standard devices with bumps density as commonly used today too.
The wafers layout will be discussed and agreed between INFN-Pisa and vendor.

Vendor should be capable to provide the full process:

- GDS layout design
- Mask preparation
- Wafer procurement
- Metal layer deposition steps
- Oxidization step and opening on passivation
- Any extra layer deposition deemed necessary by the vendor for the bump bonding technology selected and agreed with INFN-Pisa
- All steps as discussed previously for hybridization of batch-1

The number of wafers processed is planned to be small: for "ROC dummy" wafers 1-2 ROC 8-inch wafers or 2-3 6-inch wafers, for "Sensor dummy" 2-3 6-inch or 8-inch wafers.

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Bump geometry details will be discussed and agreed with INFN-Pisa in order to maximize yield and performance.

3. Single Chip assembly

3.1. General consideration on Single Chip Assembly Procedure

The assembly of the modules has the following steps:

1) Production of the masks for Bumps and UBM deposition according to the GDS files provided for batch-1 by INFN-Pisa, provided by the vendor for batch-2. This is done preliminary to the production.
2) Bump deposition and/or UBM deposition on ROC and or on Pixel sensor wafers.
   The bump center-to-center spacing is from 100 μm down to 50 μm for batch-1, 50 μm for batch-2, in the smallest dimension. The bump pattern is replicated in columns and rows on each of the ROCs and matches the same pattern on the pixel sensor.
3) Photoresist protection of the bumps, that has to be done before thinning and dicing.
4) Thinning of the ROC and sensor wafers as specified above. Thinning must include grinding defect removal and surface polishing.
5) Dicing/cutting of the ROC wafers and Pixel sensor wafers.
6) Test of the basic ROC functionality after thinning and dicing on tape. The feasibility and the procedure of this test will be discussed and agreed between vendor and INFN-Pisa.
7) Flip-chip assembly of the ROCs to pixel sensor.
8) Visual inspection and recording of inspection data at each step.
9) Each ROC after Flip Chip Bump Bonding should be X-ray inspected and recorded picture should be made available.
10) Prototypes delivery should be done with appropriate packaging (ESD safe). The packaging should be discussed with INFN-Pisa prior to shipment.

Other tests to be specified by the vendor and agreed upon by INFN-Pisa can also be performed for QA purposes.

The vendor should provide data in electronic/numeric format: in order to reveal the bump, interconnection or wafer characteristics, pairing of ROCs on Large Pixel sensors, possible ROC reworking, etc. The vendor should

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inform INFN-Pisa about possible technical problems or any other delays as early as possible.

3.1.1. Bump deposition and Flip-Chip specifications

The primary requirement for deposition of bumps (and/or UBM) on the sensor and ROC wafers is to meet the fine-pitch specification with high yield, which will allow the subsequent flip-chip assembly of the chips to the sensor with high yield of low electrical resistance connections. Details listed in the following refers to hybridization of Batch-1, specific chapter is dedicated to Batch-2.

Specific requirements are:

1) Bump material composition must be specified by the vendor and approved by INFN-Pisa. Same process for UBM, used to match the bump material and to provide high yield during flip-chip assembly, long-term high quality contacts and avoid migration of Bump material inside the wafer.
2) The process temperature profile must be specified with a maximum of 350 °C.
3) Flux less process should be used.
4) Center to center Bump pitch: 50 μm minimum.
5) The bump diameter should be not larger than 40 μm, for PROC600 to be optimized according to layout constraints.
6) Passivation opening for bump: according to point 5).
7) Alignment accuracy of flip-chip process: better than 3 μm
8) Bump height after flip-chip assembly: minimum 15 μm
9) Bump Uniformity: $\leq$ 2 μm (wafer 8")
10) Electrostatic discharge protection required during wafer handling and flip-chip assembly.
11) Additional processing on the bare module (wire bonding, gluing and component mounting) will be necessary after the hybridization. The bump deposition and flip-chip processing must be compatible with these additional assembly steps.
12) The wire bonding pads should be left clean by the process to ensure an easy and safe wire bonding with automatic equipment. Wire bonding tests, on sample, will be made on test structures from the ROC wafers before and after bumping to verify that the pads have not been degraded during the processing.

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The following points constitute additional criteria for deliverables acceptance; reference values are listed in Chapter 3 (**Acceptance Criteria**):

13) Missing or merged bump defect rate, as determined by visual inspection on a wafer, and after flip-chip assembly as determined by X-ray inspection or other means should smaller than 2% per device unit.
14) The chips should adhere firmly to the sensor after mating, and should detach only if pull force larger than 0.2 g/bump (Indium bump material) or 1.5 g/bump (other bump materials).
15) The total leakage current of a sensor must not increase too much after the dicing process. In particular the device should be operational at least up to the depletion voltage before the hybridization step.

3.1.2. Single Chip Assembly High density Bump Bonding project

The single chip assembly for Batch-2 follows similar specification listed previously for Batch-1 with the exception of following points: 4), 5), 6), 8) and 15).
Bump and UBM geometry (points 4), 5), 6) and 8)) should be optimized according to the device pitch.
The point 15) is not applicable given that we are using dummy devices.

After approval of the vendor wafer Layout the proposal for bump, UBM geometry and material will be discussed and agreed with INFN-Pisa.

3.2. Materials provided

3.2.1. By CMS

For the Batch-1 production run, INFN-Pisa will provide to the vendor:

1) Up to 6 pixel silicon sensor wafers (DWB or SOI, 150 mm diameter).
2) Up to two silicon ROC wafers (200 mm diameter).
3) Files of the wafers layout in GDS format.
4) Conceptual drawing of Benzo-Cyclo-Butene (BCB) mask.
5) KGD map for each ROC wafers and KGD map showing the good pixel sensors on the sensor wafers based on our

tests. Only the good ROC dies and pixel sensors should be used in the assembly process.

For the Batch-2 production run, INFN-Pisa will provide to the vendor:

1) Conceptual sketch agreed with the vendor, of ROC and Sensor wafer Layout

3.2.2. By Vendor

For the Batch-2 production run, the vendor will provide
1) Dummy Pixel silicon sensor wafers,(6-inch or 8-inch).
2) Dummy silicon ROC wafers (6-inch or 8-inch).
3) Files of the wafers layout in GDS format.
4) KGD dies map after optical inspection of parts.

3.3. Materials to be processed in this project

Vendor bid should be issued accordingly to the following list:

3.3.1. Batch-1 Design-A and B

Pixel wafers:
1. Units to be processed: 2 Design-A + 2 Design-B. Appropriate mask should be designed and produced.
2. Back side metallization: a uniform metal layer should be sputtered in the backside after wafer thinning. No masking is required unless this is deemed necessary by the vendor.
3. Exclusively for Design-A: a Benzo-Cyclo-Butene (BCB) protection layer should be deposited on the wafer in order to protect devices from sparks. Appropriate mask should be designed and produced.

Quotation should detail the cost for "first wafer" processed for both designs, for the "second wafers" (and for eventual more wafers beyond this offer).

ROC wafers:
4. Units to be processed: one PROC600 wafer. Appropriate mask should be designed and produced
5. BCB protection layer should be deposited on the PROC600 wafer in order to protect devices from sparks. Appropriate mask should be designed and produced.

Quotation should detail the cost for "first wafer" processed (and for eventual more wafers beyond this offer).

Flip Chip Bump bonding:

6. Devices Design-A: 28 units to be assembled
7. Devices Design-B: 40 units to be assembled

Design-A or Design-b: any extra minimal-size lot to be assembled (and for eventual more assemblies beyond this offer).

3.3.2. Batch-2

The following list is a proposal that can be discussed with vendor for points 1. and 2.

Pixel wafers:

1. Units to be processed: 2 equivalent wafers. Appropriate mask should be designed and produced

ROC wafer:

2. Units to be processed: 2 equivalent wafers. Appropriate mask should be designed and produced

Flip Chip Bump bonding:

3. Units to be assembled: 20 units to be assembled
4. Any extra minimal-size lot to be assembled (and for eventual more assemblies beyond this offer).

For Batch-1 and Batch-2 INFN-Pisa reserves the right to order additional Flip-chip at the same unit price and conditions as stated in the vendor bid, provided that the purchase option for additional modules does not imply processing of new wafers.

3.4. Other Details to be Included in the Vendor bid

The vendor should provide to INFN-Pisa detailed information such as the temperature under which the bumping process, including UBM deposition, will be carried out and its duration in time, the UBM thickness and metal type that will be used.

The vendor should inform INFN-Pisa of their dicing tolerance, preferably with illustrative photographs and/or statistical data, and whether they will do the dicing in-house or if this will be sub-contracted. If a sub-contractors will be used in any phase of the work this should be clearly indicated in the bid, including the names of the sub-contractor(s).

3.5. Shipping and Packaging

The vendor is going to deliver assembled pixel bare modules to the final destination CERN Route de Meyrin 385, 1217 Meyrin (CH) or CERN F01631 Prevessin CEDEX (Fr) site for EU vendors. The vendor should consult INFN-Pisa about the packaging of the parts before delivery.

4. Processing Schedule and Quality Assurance

4.1. Introduction

This chapter covers the estimated timeline for wafer project and the quality assurance (QA) plan for the silicon pixel sensors Hybridization.

4.2. Timelines for Wafer Processing

Kick-off of the project is foreseen after contract is issued and material is delivered to the company.
The production can be scheduled in sub-lots regularly delivered by month basis, upon request of INFN and agreement with the vendor.
The **production kick-off** for each batch is defined by the arrival of the materials from INFN-Pisa and/or agreement between INFN-Pisa and vendor about mask designs.

The preliminary proposal for delivery follows:

- Batch 1 Design-A can be scheduled in 2 sub batches
  - First sub batch should be processed and delivered within 12 weeks from **production kick-off**
  - Production should last a maximum of **12 months**
- Batch 1 Design-B can be scheduled in 4 sub batches
  - First sub batch should be processed and delivered within 12 weeks from **production kick-off**
  - Production should last a maximum of **12 months**
- Batch 2 can be scheduled in 2 sub batches
  - First sub batch should be processed and delivered within 18 weeks from **production kick-off**
  - Batch 2 production should last a maximum of **12 months.**

Delivery of batches as scheduled will allow a better management of the production and eventual feedback to vendor if production issues are detected as explained in the following chapter.

4.3. Quality Assurance

In order to ensure consistent quality throughout the hybridization process, the following steps will be taken:

- A monthly status report will be submitted to INFN-Pisa to summarize the project status.
- During the processing of each device data is recorded in a vendor's lot tracking system about critical feature dimensions, film thicknesses, bump heights, etc. This data will be provided to INFN-Pisa during lot processing as part of the report, and any issues will be discussed.
- Tracking of ROC die bonded to device will be recorded on appropriate maps as provided by INFN-Pisa.
- All documents should be made available in electronic format upon agreement between INFN-Pisa and vendor.

5. Acceptance Criteria

5.1. Overview

This chapter summarizes the **Acceptance Criteria** for the assembled parts and the **Evaluation Criteria** for the procurement.

Configuration and technical specification are detailed in the chapters 1 to 3 of the **Technical Specification** document.

The present devices assembled by the vendor will be injected in a chain of assembly steps that will assess the quality according to the number of pixel defect per device and the total current measured at operating voltage.

5.2. ACCEPTANCE CRITERIA

The goals of the Project are:

- **to obtain the required number of adequately functioning assembled devices with the fewest defective interconnections and the least waste of ROCs and Sensors for the best price;**
- **to select a vendor that can meet our delivery schedule.**

The present hybridization project will be monitored at level of devices upon reception at INFN-Pisa laboratory. In order to meet the condition for the majority of the devices to be classified as accepted, or category "A", we are using a set of acceptance criteria for the hybridization step listed in the following.

In this section we describe how we will determine that a vendor can produce modules with an acceptable yield and explain the Figure of Merit we will use to evaluate bids.
All inspections, mechanical and electrical tests described below will be performed by the **INFN-Pisa** upon reception.

Vendor should be able to meet the following requirements

The Requirements are:

R.0 The vendor should setup a QA plan, to be supplied in the vendor bid. Specifically, the document should include:

a. QA method to ensure lot-to-lot consistency.

b. Description of X-ray and pull tests facilities and procedures.
c. Format of data to be provided to INFN-Pisa.
d. Method allowing INFN-Pisa to track the status of the processing.
e. Monthly status report document proposal.

We will NOT ACCEPT vendor bid without QA plan as requested.

R.1 The vendor should setup a production plan, to be supplied in the vendor bid. Specifically, the document should include the Production and delivery schedule.
In general, we will NOT ACCEPT vendor bid with production plan:

a. Longer than 12 months.
b. Having a production rate conflicting the one proposed in this document.

For item a. delays due to INFN-Pisa will not be accounted in the total time figure.

R.2 In general, we will NOT ACCEPT Bump-Bonded modules with one of the conditions listed below:

a. chipped edges;
b. broken/cracked chips or sensor;
c. unusable wire bonding pads.

For items a. and b., non-compliance is established by picture documented visual inspection. Most external implant in the periphery should be at least 30 microns away from the kerf edge. The dicing tolerance is ±20 microns. The kerf width should be less than 50μm. Dicing should be done with a saw compatible with these specifications. The grit/concentration used should agree with the industrial standard for dicing silicon. De-ionized water should be used during dicing.
For item c. the wire bonding pads should allow wire bonding with a standard automatic machine. Wire bonding tests, on samples, will be made on test structures from the ROC wafers before and after bumping to verify that the pads have not been degraded during the processing.

Furthermore, the following requirements must be met (all modules must satisfy all the requirements, except for "pull strength," criterion R.4 below):

R.3 The mechanical tolerances listed in the **Device specification** chapter must be met:

1) Center to center Bump pitch: 50 μm minimum.

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2) The bump diameter should be not larger than 40 μm.
3) Passivation opening for bump: according to point 2)
4) Alignment accuracy of flip-chip process: better than 3 μm
5) Bump height after flip-chip assembly: minimum 15 μm

R.4 The pull strength of the ROC should be no less than 0.2 g/bump in case of Indium bumps and no less than 1.5 g/bump for other bump materials.
This will be determined by testing (at room temperature: 20°C) on a few parts, by sampling on good modules or on modules that failed one of the electrical tests.

Following points (R.5-R.6) should be applied to batch-1 only.

R.5 The Pixel devices from the KGD maps meet a set of electrical specifications upon delivery. The same specifications must be met post hybridization. The total leakage current of a sensor must not increase too much after the dicing process. In particular the device should be operational at least up to the depletion voltage before the hybridization step. In case of non-compliance investigation must be undertaken together by INFN-Pisa and vendor in order to solve issues.

R.6 The ROCs from the KGD maps meet a set of electrical specification upon delivery. The same specification must be met post hybridization. In particular:

R.6.1 All ROCs on the bump-bonded module are functional (can be powered on and off, registers/DACs can be loaded, data can be readout). This test will be performed at room temperature.

R.6.2 The number of bumps missing, bridged, or failing electrical tests at room temperature must be fewer than 100 on any ROC (~2.5%), in addition to the bad pixels already identified at delivery to the vendor. This test will be performed on devices after assembly.

In order to meet quality cuts applied in **R.6** single ROC chip reworking can be performed:

R.6.3 single chip reworking made by vendor should be notified to INFN-Pisa and documented.

R.6.4 single chip reworking can be performed also upon INFN-Pisa request after QA test.

R.7 Modules failing the test criteria listed in this section will be rejected. The ratio between good Flip chipped modules produced and good sensors received define the yield, Y and the inefficiency (1-Y).

5.3. EVALUATION AND CONTRACT MONITORING

5.3.1. Rules for Quotation analysis and Awarding of the contract.

The quotation will be evaluated according to **qualitative** and **quantitative** criteria. A total of 100 points score are available for the evaluation.

The **qualitative** criteria consists on the accomplishment of the requirements:
R.0, the score assigned is equal to **20** points. For this qualitative criterion each committee member will assign a coefficient indicating the level of compliance with the requested specifications, using as a guide the following scale:

The QA plan does not meets the requirements. Unacceptable	0
The QA plan is almost absent. Almost unacceptable.	0.1
The QA plan is very poorly presented.	0.2
The QA plan is poorly presented.	0.3
The QA plan does not present technical details, with few points missing. Unremarkable	0.4
The QA plan does not present technical details, with one point missing. Somewhat expected	0.5
The QA plan does not present technical details. Acceptable	0.6
The QA plan all points answered good	0.7
The QA plan all points with partial techincal detail. Very good	0.8
The QA plan all points with 1 missing item detail. much better than expected	0.9
The QA plan is well discussed in requirements and technical details	1

The individual committee members coefficients are averaged to obtain the un-normalized committee coefficient for a specific criterion and a specific quotation. Finally, for each criterion, the un-normalized committee coefficients of the various quotations are divided by the maximum coefficient scored by any quotation for that criterion, obtaining the final coefficients, normalized to 1, as prescribed from "Linee Guida ANAC n. 2

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recanti: offerta economicamente più vantaggiosa approvate dal Consiglio di Autorità con Delibera n.1005 del 21 Settembre 2016"[1]

For the **quantitative** evaluation we have reserved **80** points score, and the quotation will be evaluated by providing a Figure of Merit, through a weighted sum of criteria and goals as detailed below.
The vendor with the highest figure of merit and who can meet the proposed schedule will be awarded of the contract.

The Figure of Merit is calculated by the following formula

$$FM = \sum_{1}^{n} (Max\ score)_i W_i V_i$$

where ***Max score*** is the value in points per criterion; the sum of all **Max scores** is equal to **80**. W_i is the weight for the coefficient V_i assigned to each criterion.

Each V_i is evaluated by comparing the current offer with the "best" offer as explained in the following

We define the following criteria:
V_1 "cost of the project" (max score=**60** points)
V_2 "delivery time" (max score=**20** points)

Definition of V_1 cost of the project and W_1
Project Cost has the following evaluation: we consider ***C*** the percentage of reduction of the C_{OFF} current offered cost compared to the C_{INFN} foreseen cost $C=(C_{INFN} - C_{OFF})/C_{INFN}$.

The V_1 is defined as $V_1=C/C_{max}$ where C_{max} is the highest percentage of reduction offered.

The weighting factor W_1 is equal to 1.

Definition of V_2 Delivery Time and W_2
Previous experience shows that the hybridization process request is compatible with a delivery time of T_n=12 months.

[1]The document (in Italian) is available for download at the following web address: http://www.anticorruzione.it/portal/public/classic/AttivitaAutorita/AttiDellAutorita/_Atto?ca=6605

Given T_c the current vendor quoted delivery time, we consider the reduction of the delivery time $\Delta T_c=(12-T_c)$: R_c percentage of reduction of ΔT_c compared to T_n
The V_2 is defined as $V_2=R_c/R_{max}$ where R_{max} is the highest percentage of reduction offered.

The weighting factor W_2 is equal to 1.

5.3.2. Quality Assurance in production

We will monitor the quality of the assembly by measuring the Yield on the received modules. The Yield is evaluated on the bases of the delivery and INFN-Pisa will provide feedback within one week to the vendor on the results and help to solve problems.

Contract Technical Clauses and breakdown of Penalties, intended as integration of the Contract Clauses document.

In the event of non-performance or improper performance of the contract the vendor will be charged a penalty with criteria detailed in the following.

TC0: If the schedule slips by one month and if the production rate is not recovered within next month
Penalty is equal to 2% of the contract.

TC1: If the production Yield should fall below 50% for a sub-lot delivered,
Penalty is the following: the vendor should produce more modules to reach at least 50% the sub-lot initial request without additional costs.

TC2: Once agreed upon, any proposed change with respect to the approved Production and QA Plan during the Production Phase must be subject to prior approval by INFN-Pisa in writing.
In case of not observance the Penalty is equal to 2% of the contract.