Lotto A - Flip Chip Assembly for the PixFEL single chip detector

Technical specifications

INFN – Pisa

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1. Introduction

This document is the basis for the tender for flip chip assembly of the PixFEL detector demonstrator, to be realized with an hybridization process among sensors and ROC chips only available as single die. In this first section a general introduction to the PixFEL project and an overview of the PixFEL detector demonstrator will be given. In section 2 the technical specifications for the device will be detailed, while in section 3 the requirements on delivery, installation and verification will be explained. Finally, in section 4 the criteria that will be used for the evaluation of the bids and for awarding the contract will be discussed.

1.1. Introduction to the PixFEL Project

The PixFEL project, funded by the INFN, is the first stage of a long term research program aiming at the development of advanced X-ray imaging instrumentation for applications at the free electron laser (FEL) facilities. The project aims at substantially advancing the state-of-the-art in the field of 2D X-ray imaging by the exploration of cutting-edge solutions for fabrication technologies and detector readout architecture design. The PixFEL collaboration plans to improve the performance of current imaging systems in several areas: reduce pixel pitch while retaining high speed readout and local frame storage; retain large dynamic range with high resolution in-pixel analog-to-digital conversion; keep minimal module dead areas allowing large area tiling without missing data issues.

An overview of the proposed PixFEL X-ray imager is given in Figure 1, that shows a matrix (part of a more complex and larger area detection system) of 9 four-side buttable blocks, each consisting of a multilayer device: a fully depleted high resistivity active edge pixel sensor bump bonded to a dual tier front-end chip. The chip, in turn, is interconnected to a hybrid board. Design of the building blocks and of the readout architecture will be carried out in a 65 nm CMOS technology that enables the implementation of the required amount of on-board intelligence in a target pitch of about 100 μm, including in-pixel analog-to-digital conversion and data storage.

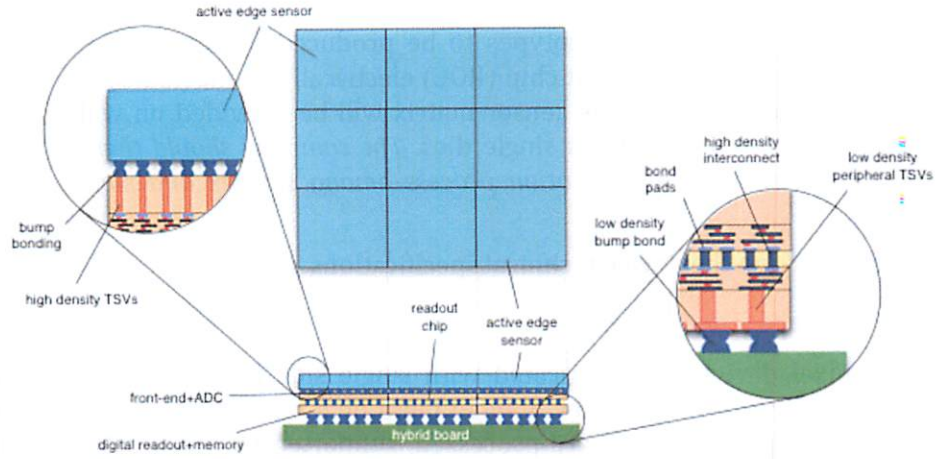
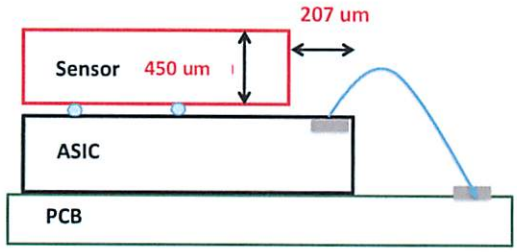


Figure 1: Conceptual view of a 3x3 detector matrix made of 9 four-side buttable elementary blocks.

1.2. Overview of the PixFEL demonstrator

At the end of the first 3 years of activity the PixFEL project plan to produce a first demonstrator for the X-ray imager (which, in this first phase, will not include the memory layer) composed by a single tier 32x32 channels readout chip (**ROC**) interconnected by bump bonding to a fully depleted active edge pixel sensor matrix, as shown schematically in Figure 2.



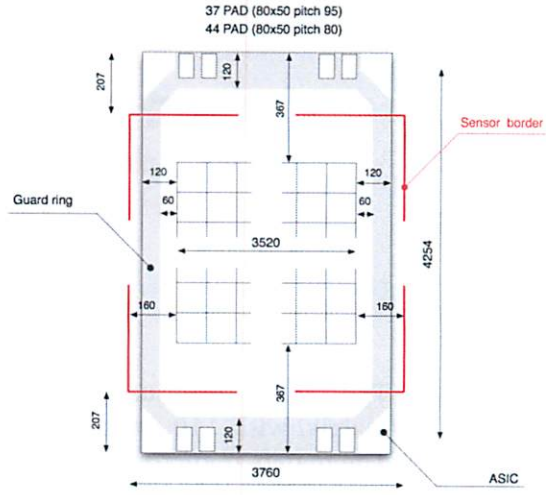


Figure 2: Conceptual scheme of the PixFEL demonstrator

The ROC chips and the pixel sensor matrix have been already produced by the collaboration and are currently under tests. A final test of the sensor – ROC assembly with X-ray and radioactive sources will prove the full functionality of the device. The company should supply 10 single chip module assembled.

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2. Device technical details

The basic unit of the prototypes to be produced by the company is a device which consists of a readout chip (ROC) electrically connected by bump-bonds to a pixel silicon sensor. The sensor matrix will be provided on wafers, while the ROCs are only available as single dies. *The company should then have a proven track record with hybridization process among sensors and single die readout chips.*

In this section the device technical specifications are detailed.

2.1. Sensor description

The pixel devices are fabricated with single side process on 6-inch diameter silicon-silicon Directs Wafer Bonded build by a high resistivity n-type wafer, in which the pixel unit cell are processed, supported by a low resistivity support wafer, (Figure 3). The support wafer is needed since the sensor is surrounded by trenches filled by poly-Si extending extending through all the active thickness. The support wafer is 250 um thick while the sensor wafer is 450 um thick.

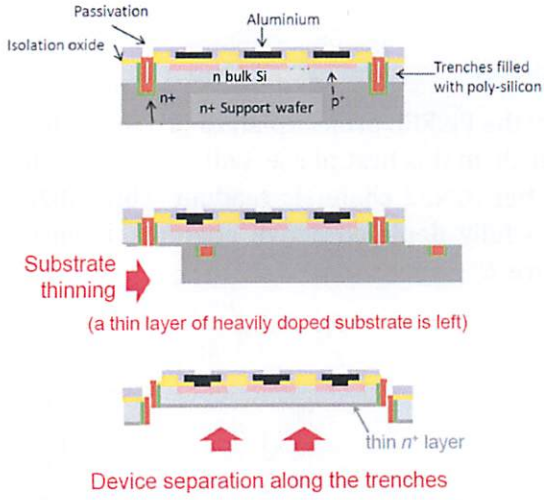

Figure 3: Cross section of active edge sensor wafer

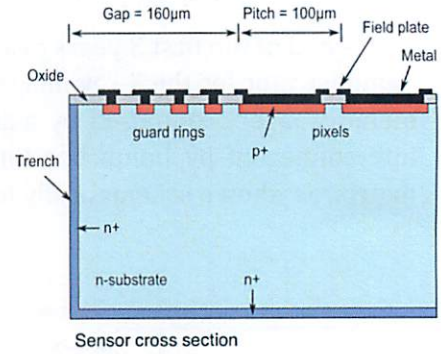

Figure 4: Matrix sensor cross section

The sensor to be used for the assembly is a 32x32 p+ on n active edge pixel matrix, with 110 um x 110 um pixel pitch, processed with planar technology. The matrix is surrounded by four p+ implanted guard rings and by the trenches, as shown in Figure 4 and 5. The external dimension of the sensor chip are 3.815 mm x 3.815 mm.

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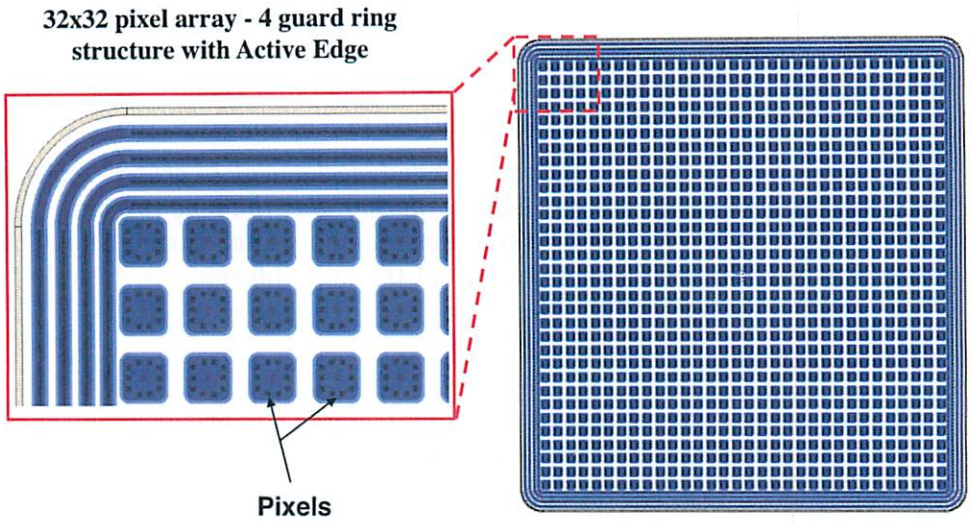

Figure 5: 32x32 pixel array

The layout of the full 6-inch wafer, shown in Figure 6, includes several different pixel arrays and test structures. Each wafer hosts 18 sensors of the type be used for the assembly, localized in region B18.

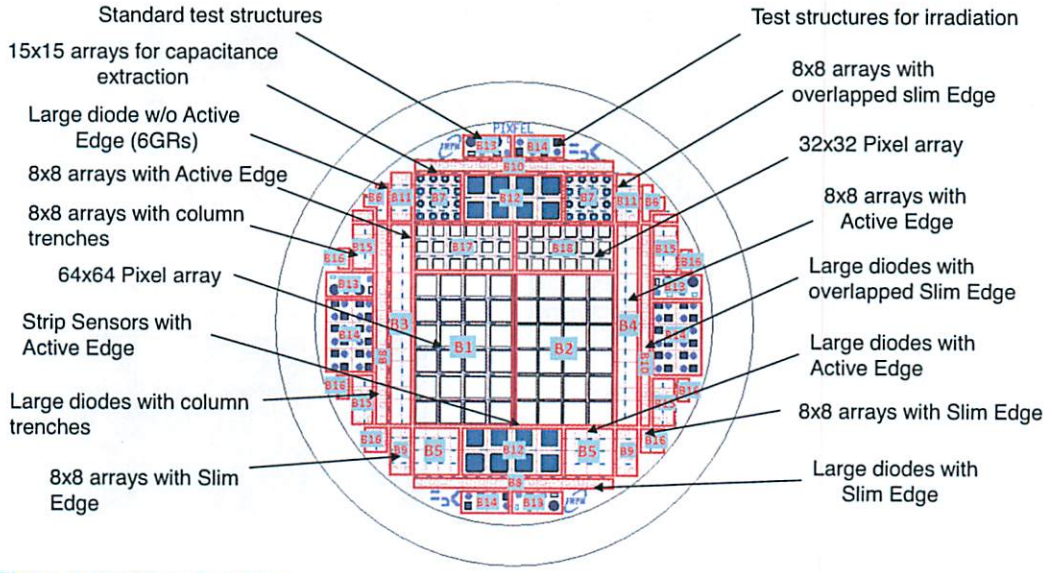

Figure 6: PixFEL wafer layout

The INFN will provide the GDS file of the sensor's layout needed to design the mask for Under Bump Metal deposition (UBM) on solder pads and alignment mark structures on the sensors. Three wafers (2+ 1 spare) will be supplied by the INFN and a map of the sensors to be used will be also provided.

2.2. Thinning of the Pixel Sensors wafers & sensor matrix separation

After the process steps needed for solderable pad deposition on the sensor matrix, and before the connection to the ROC, the backside 250µm-support wafer

needs to be removed. The wafer will be thinned, by grinding, to about 450 μm, according to INFN prescription for the final thickness. After thinning the single active edge 32x32 pixel matrix need to be separated (Figure 3), inspected and stored into carriers (GelPack) before further processing steps.

The vendor has to take precautions, ESD and mechanical, to protect the wafer and the solder pads against any damage during the thinning process (chipping, cracking, or shattering). All sensor wafer remnants after cutting should be sent back to INFN-Pisa with their individual tracking information, including wafer number and position in the wafer.

2.3. ROC description

The PixFel ROC (PFM2) chip is a readout integrated circuit, consisting of 32×32 square cells. It has been designed in a TSMC 65 nm CMOS technology and is currently under test. The die covers an area of 4.324×3.830 mm^2 (including seal ring).

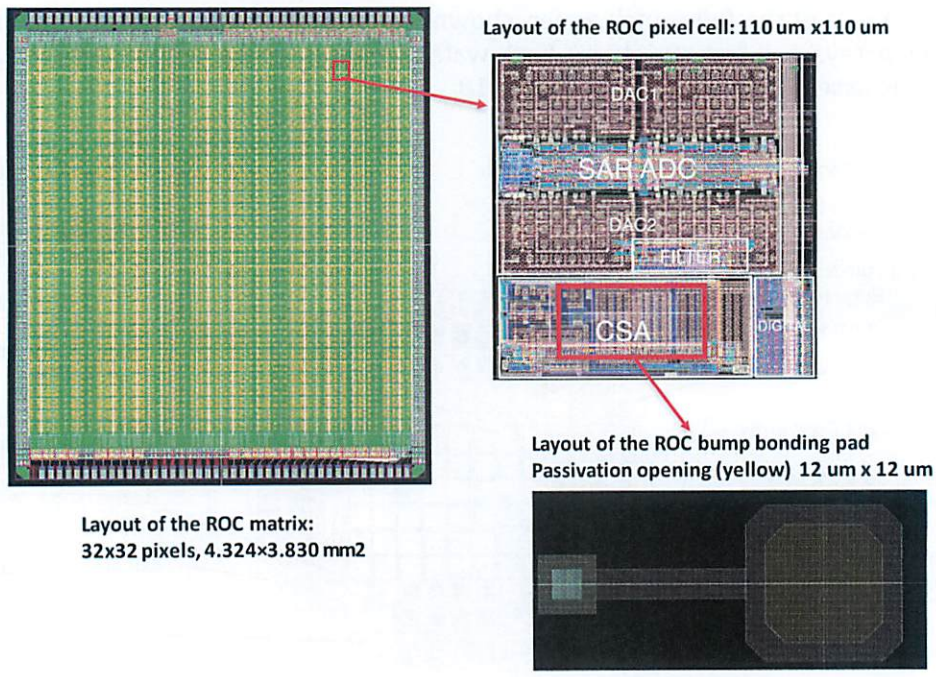

Figure 7: PFM2 ROC layout

The pixel cell covers an area of 110×110 μm^2. The analog front-end of each pixel includes a Charge Sensitive Amplifier (CSA), a time variant filter and an Analog-to-Digital Converter.

The layout view of the chip is shown in Figure 7, where is also visible the detail of a single pixel cell, and the pad designed for the bump bonding with the sensor matrix. The passivation bump opening is 12 um x12 um and passivation thickness is approximately 1 um.

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Beside the 32×32 matrix of pixels, other peripheral blocks are included in the chip. Moreover, two rows of wire bonding pads are distributed on the top and bottom side of the chip. *These wire bonding pads should not be affected by the hybridization processing.*

Since the chips have been produced in MPW they are available only as single dies and they should be embedded in a ceramic carrier wafer for the hybridization process. *The company should then have a proven track record in hybridization process among sensors and single die ROC chips.*

The vendor has to take precautions, ESD and mechanical, to protect the ROCs against any damage during the process (chipping, cracking, or shattering)

The INFN will provide the GDS file of the ROC's layout, needed to design the mask for bumps/UBM and alignment mark structures for the carrier wafer of the ROC chip.

2.4. Process steps for single chip Assembly Procedure

The main process steps for the hybridization process of the single chip device are the following:

1. Design and mask preparation:
- Preparation of gds2 bumping mask for single ROC chip carrier wafer (bump structures, alignment marks)
- Preparation of gds2 UBM mask for sensor wafer (UBM pad structures, alignment marks)
- 5" mask preparation for carrier wafer
- 7" mask preparation for sensor wafer

2. Wafer and chip process:
- Sensor wafer:
    - UBM deposition on sensor wafer
    - Backside carrier wafer removal (grinding/polishing, stop at pre-defined thickness)
    - Sensor chip separation and sorting
- Readout chips:
    - Measurement of the X-Y dimensions of the ROC chips
    - Preparation of carrier wafer and chip attach
    - Solder bumping of readout chip
    - Demounting from carrier wafer (dicing)
    - Cleaning

3. Flip chip assembly:
    - Pick and place of readout chip onto sensor chip
    - Reflow soldering
    - x-ray inspection and documentation
    - shipment to INFN

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2.5. Bump Deposition and Flip-Chip specifications

The primary requirement for deposition of bumps (and/or UBM) on sensor and ROCs is to meet the fine pitch specification with high yield, which will allow the subsequent flip-chip assembly of the chips to the sensor with high yield of low electrical resistance connections. Specific requirements are:

1. Ability of the company to perform hybridization process among sensors and single die ROC with high yield
2. Alignment accuracy of flip-chip process better than 3 um
3. Bump height after flip-chip assembly between 15 and 40 um
4. Bump uniformity better or equal to 2 um
5. Ability to supply complete information about x-ray inspection of the assembly after flip-chip process, needed to access the quality of the device.
6. Bump material composition must be specified by the vendor and approved by INFN. Same process for UBM, used to match the bump material and provide high yield during flip-chip assembly, long-term high quality contacts and avoid migration of bump material inside the wafer.
7. The process temperature profile must be specified
8. Flux less process should be used
9. Electrostatic discharge protection required during wafer handling and flip-chip assembly
10. Additional processing on the assembled device (wire bonding, gluing and mounting) will be necessary after hybridization. The bump deposition and flip-chip processing must be compatible with these additional assembly steps.
11. The wire bonding pads should be left clean by the process to ensure an easy and safe wire bonding with automatic equipment.
12. *The vendor has to take precautions, ESD and mechanical, to protect the sensors and ROC chips against any damage during the process (chipping, cracking, or damaged wire bonding pads)*

2.6. Material provided by INFN

- Sensor wafer:
  - 32x32 pixels silicon sensors with 110µm pitch on 6'' wafers (2 +1 spare wafers);
  - Sensor wafer 450µm active thickness and are bonded to a 250µm support wafer
  - Sensors have an active edge with trenches extending through all the active thickness
  - The support wafer needs to be removed after processing
  - Gds2 layout file of top metal and passivation layer
- Readout Chip:
  - 10x ROICs with an area around 4 mm x 4 mm, available as singulated dies (number of final assemblies 10 + 2 spares);
  - Gds2 layout file of top metal and passivation layer (single readout chip)

2.7. Material to be process by the vendor

- Design and produce 7 inches glass mask for UBM and alignment mark structures for the sensor wafer.
- Design and produce 5 inches glass mask for bumps/UBM and alignment mark structures for the carrier wafer of the ROC chip.
- Process 2 (+1) pixel sensor wafers as described in section 2.4
- Process 10 (+2) ROC chips as described in section 2.4
- Flip chip assembly of 10 (+ 2) single chip modules as described in section 2.4

2.8. Other details to be included in the bid

The vendor should provide INFN-Pisa with detailed information such the temperature under which the bumping process, including UBM deposition, will be carried out and its duration in time, the UBM thickness and metal type that will be used. If a subcontractor will be used in any phase of the work this should be clearly indicated in the bid, including the names of the sub-contractor(s).

2.9. Shipping and packaging

The vendor is going to deliver assembled device to INFN-Pisa.

The vendor should consult INFN-Pisa about the packaging of the parts before delivery.

3 Delivery and verification

3.1 Quality control during production

During the process of each device data is recorded in a vendor's lot tracking system about critical feature: x-ray inspection data, dimensions, thickness, bump heights etc. Tracking of ROC die bonded to device will be recorded by the vendor. All documents should be made available in electronic format upon agreement between INFN-Pisa and the vendor.

3.2 Delivery Time

Kick-off of the project is foreseen after contract is issued and material is delivered to the company.

The full assembly process should last 5 months.

The sensor - ROC assembly should be delivered to the INFN-Pisa.

3.3 Verification and certification

Within 1 month from delivery, the assemblies will be subject to a verification and certification by INFN personnel, who will test the system against the stated specifications. In general we will NOT ACCEPT bump bonded modules with one of the conditions listed below :

- Chipped edges
- Broken/cracked chips or sensor
- Unusable wire bonding pads

Only the positive verification and certification will authorize the full contract payment by INFN.

4 Minimal requirements to participate to the bid

Vendors can participate to the bid only if they can supply:

- *a proved ability to perform hybridization process among sensors and single die ROC with high yield following the specification detailed in Sec. 2.5*

5 Bid evaluation criteria

The quotation will be evaluated on the basis of a figure of merit (FM) that combines the production time and the cost as described below.

5.1 Rules for quotation evaluation and contract awarding

The quotation figure of merit FM(q) is calculated combining a number N of criteria according to the following formula:

$$FM(q) = \sum_{i=1}^{N} W_i V_i(q)$$

where:

- W_i are the weights assigned to each criterion, with a total of $\sum_i W_i = 100$;
- $V_i(q)$ are the calculated or evaluated coefficients for each criterion for the quotation q with $0 \leq V_i(q) \leq 1$

Two types of criterion calculation are possible: qualitative and quantitative.

We define the following criteria:

Criterion	Description	Type	Weight
C.1	Delivery time	Quantitative	20
C.2	Cost	Quantitative	80

C.1 Delivery time

The delivery time value $A(q)$ of each quotation is calculated as the percent reduction with respect to the base tender delivery requirement. The maximum quotation value A_{MAX} is then calculated and the individual coefficients calculated as follows:

$$V_3(q) = A(q)/A_{MAX}$$

C.2 Cost

The cost coefficient calculation proceeds as follows. The value of each quotation $A(q)$ is calculated as the percent reduction with respect to the base tender cost, so that a quotation with lower cost has a higher value. The maximum and

average quotation values are then computed, A_{MAX} and A_{AVG}, and the individual coefficients calculated as follows:

If $A(q) \leq A_{AVG}$	$V_2(q) = XA(q)/A_{AVG}$
If $A(q) > A_{AVG}$	$V_2(q) = X + (1 - X)(A(q) - A_{AVG})/(A_{MAX} - A_{AVG})$

with X = 0.9.

5.2 Option to purchase additional assemblies

INFN reserves the right to order additional modules, at the same unit prices and conditions as stated in the vendor bid, provided that the purchase option for additional modules is taken up by INFN not later than 2 months after the contract award. The cost of additional modules will not exceed 30% of the initial tender cost.