

**GIUNTA ESECUTIVA**

DELIBERAZIONE N. 11204

La Giunta Esecutiva dell'Istituto Nazionale di Fisica Nucleare, riunita in Roma in data 16.11.2016

- vista la nota del 25.10.2016, con la quale il Dr. Marco Grassi, Direttore della Sezione di Pisa, chiede l'indizione di una procedura per la realizzazione dell'interconnessione tramite flip-chip bonding del chip di readout e del sensore per il successivo test con sorgenti e su fascio per l'esperimento PixFEL e per la costruzione dei rivelatori a pixel di silicio necessari ad equipaggiare il prossimo rivelatore a pixel di CMS previsto per l'upgrade di Fase II nell'ambito dell'esperimento RDFASE2, distinta in due lotti;
- preso atto che le funzioni di Responsabile Unico del Procedimento sono espletate dal Dr. Roberto Dell'Orso;
- considerato che per l'acquisto della fornitura sopra descritta è possibile espletare una procedura negoziata previa consultazione, con avviso a manifestare interesse, con il criterio dell'offerta economicamente più vantaggiosa, individuata sulla base del miglior rapporto qualità/prezzo, ai sensi degli artt. 36 co. 2 lett. b) e 95 co. 2 del d.lgs. n. 50/2016, con attribuzione di massimo punti 20 all'offerta tecnica e massimo punti 80 all'offerta economica per il Lotto A e con attribuzione di massimo punti 20 all'offerta tecnica, massimo punti 60 al prezzo e massimo punti 20 alla riduzione dei tempi di consegna per il Lotto B;
- preso atto che la valutazione delle offerte sarà effettuata utilizzando le seguenti formule:

Lotto A

- per la valutazione della riduzione dei tempi di consegna: la formula del ribasso indicata nel paragrafo 5.1, punto C.1 del Capitolato Tecnico;
- per la valutazione dell'offerta economica: la formula del ribasso indicata nel paragrafo 5.1, punto C.2 del Capitolato Tecnico, contenente il valore soglia;

Lotto B

- per la valutazione della riduzione dei tempi di consegna: la formula del ribasso indicata nel paragrafo 5.3.1 del Capitolato Tecnico;
- per la valutazione degli elementi qualitativi: la media dei coefficienti attribuiti discrezionalmente da parte di ciascun commissario;
- per la valutazione dell'offerta economica la formula del ribasso indicata nel paragrafo 5.3.1 del Capitolato Tecnico;

- visti il Capitolato tecnico e le Condizioni contrattuali, predisposti dal Responsabile Unico del Procedimento, allegati alla presente deliberazione come parti integranti e sostanziali;
- preso atto che per la fornitura in argomento è stimata una spesa di € 78.278,68, di cui oneri relativi a rischi da interferenze pari a zero, oltre IVA 22%, per un totale di € 95.500,00, che troverà copertura nel bilancio 2016 dell'Istituto - capitolo U1030102008 - come segue:
  - lotto A: € 31.500,00, di cui oneri per eliminazione rischi da interferenze pari a zero IVA inclusa (esp. PixFEL- CSNV);
  - lotto B: € 64.000,00, di cui oneri per eliminazione rischi da interferenze pari a zero IVA esente per consegna al CERN (esp. RDFASE2);
- preso atto che la presente fornitura non è prevista negli strumenti Consip del Programma di razionalizzazione degli acquisti della P.A.;
- considerato che, ricorrendo le condizioni di cui all'art. 52 co. 1 lett. c) del d.lgs. 50/2016, nelle more dell'acquisizione delle attrezzature specializzate per l'utilizzo dei mezzi di comunicazione elettronici, è consentito richiedere la presentazione dell'offerta in forma non elettronica;
- vista la deliberazione del Consiglio Direttivo n. 11190 del 29.10.2009, pubblicata sulla G.U. n. 55 del 08.03.2010, che fissa in 180 giorni dall'avvio della procedura la durata massima del procedimento di selezione del contraente negli appalti pubblici;
- vista la deliberazione dell'Autorità Nazionale Anticorruzione (ANAC) del 22.12.2015, in attuazione dell'art. 1, commi 65 e 67 della legge 266/05;
- visto l'articolo 14 co. 5 dello Statuto dell'INFN, secondo cui la Giunta Esecutiva delibera in materia di contratti per lavori, forniture e servizi e prestazioni d'opera e professionali che esulano dalla competenza dei Direttori delle Strutture.

## **DELIBERA**

1. Di approvare il Capitolato tecnico e le Condizioni contrattuali, predisposti dal Responsabile Unico del Procedimento, che costituiranno la base documentale per la procedura di gara per la realizzazione dell'interconnessione tramite flip-chip bonding del chip di readout e del sensore per il successivo test con sorgenti e su fascio per l'esperimento PixFEL e per la costruzione dei rivelatori a pixel di silicio necessari ad equipaggiare il prossimo rivelatore a pixel di CMS previsto per l'upgrade di Fase II nell'ambito dell'esperimento RDFASE2, distinta in due lotti di gara.
2. Di indire una procedura negoziata previa consultazione, con avviso a manifestare interesse, con il criterio dell'offerta economicamente più vantaggiosa, individuata sulla base del miglior rapporto qualità/prezzo, ai sensi degli artt. 36 co. 2 lett. b) e 95 co. 2 del d.lgs. n. 50/2016, con attribuzione di massimo punti 20 all'offerta tecnica e massimo punti 80 all'offerta economica per il Lotto A e massimo punti 20 all'offerta tecnica, massimo punti 60 al prezzo e massimo punti 20 alla riduzione dei tempi di consegna per il Lotto B.

3. Di imputare la spesa stimata di € 78.278,68, di cui oneri relativi a rischi da interferenze pari a zero, oltre IVA 22%, per un totale di € 95.500,00, nel bilancio 2016 dell'Istituto - capitolo U1030102008 - come segue:
  - lotto A: € 31.500,00, di cui oneri per eliminazione rischi da interferenze pari a zero IVA inclusa (esp. PixFEL- CSNV);
  - lotto B: € 64.000,00, di cui oneri per eliminazione rischi da interferenze pari a zero IVA esente per consegna al CERN (esp. RDFASE2).
4. Di incaricare il Presidente di nominare, con propria disposizione, i componenti la Commissione Giudicatrice.

# Lotto A - Flip Chip Assembly for the PixFEL single chip detector

## Technical specifications

INFN – Pisa

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## 1. Introduction

This document is the basis for the tender for flip chip assembly of the PixFEL detector demonstrator, to be realized with an hybridization process among sensors and ROC chips only available as single die. In this first section a general introduction to the PixFEL project and an overview of the PixFEL detector demonstrator will be given. In section 2 the technical specifications for the device will be detailed, while in section 3 the requirements on delivery, installation and verification will be explained. Finally, in section 4 the criteria that will be used for the evaluation of the bids and for awarding the contract will be discussed.

### 1.1. Introduction to the PixFEL Project

The PixFEL project, funded by the INFN, is the first stage of a long term research program aiming at the development of advanced X-ray imaging instrumentation for applications at the free electron laser (FEL) facilities. The project aims at substantially advancing the state-of-the-art in the field of 2D X-ray imaging by the exploration of cutting-edge solutions for fabrication technologies and detector readout architecture design. The PixFEL collaboration plans to improve the performance of current imaging systems in several areas: reduce pixel pitch while retaining high speed readout and local frame storage; retain large dynamic range with high resolution in-pixel analog-to-digital conversion; keep minimal module dead areas allowing large area tiling without missing data issues.

An overview of the proposed PixFEL X-ray imager is given in Figure 1, that shows a matrix (part of a more complex and larger area detection system) of 9 four-side buttable blocks, each consisting of a multilayer device: a fully depleted high resistivity active edge pixel sensor bump bonded to a dual tier front-end chip. The chip, in turn, is interconnected to a hybrid board. Design of the building blocks and of the readout architecture will be carried out in a 65 nm CMOS technology that enables the implementation of the required amount of on-board intelligence in a target pitch of about 100  $\mu\text{m}$ , including in-pixel analog-to-digital conversion and data storage.

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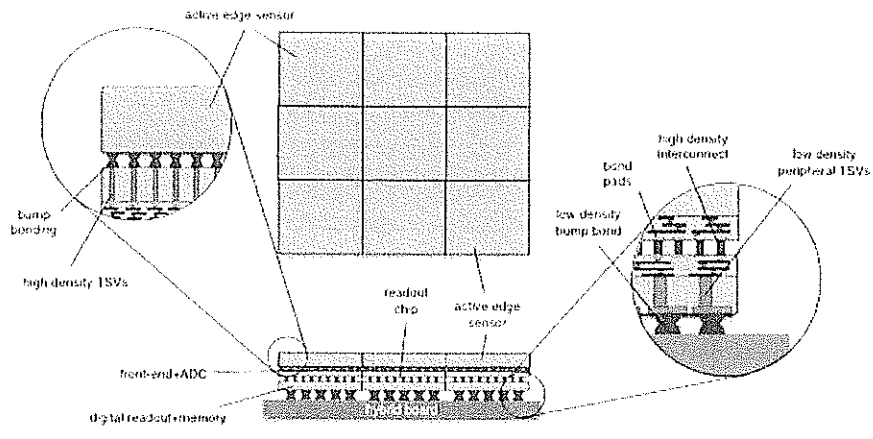


Figure 1: Conceptual view of a 3x3 detector matrix made of 9 four-side butttable elementary blocks.

1.2. Overview of the PixFEL demonstrator

At the end of the first 3 years of activity the PixFEL project plan to produce a first demonstrator for the X-ray imager (which, in this first phase, will not include the memory layer) composed by a single tier 32x32 channels readout chip (ROC) interconnected by bump bonding to a fully depleted active edge pixel sensor matrix, as shown schematically in Figure 2.

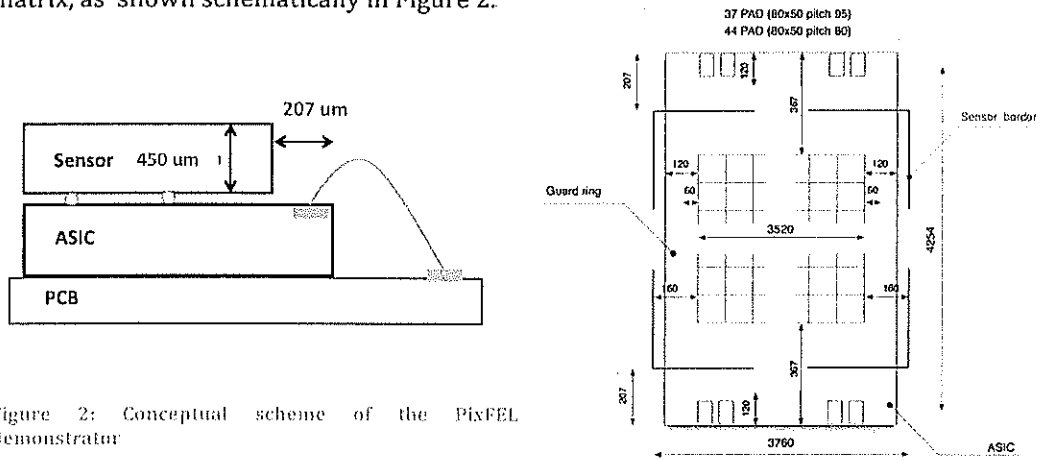


Figure 2: Conceptual scheme of the PixFEL demonstrator

The ROC chips and the pixel sensor matrix have been already produced by the collaboration and are currently under tests. A final test of the sensor – ROC assembly with X-ray and radioactive tests will prove the full functionality of the device. The company should supply 10 single chip module assembled.

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2. Device technical details

The basic unit of the prototypes to be produced by the company is a device which consists of a readout chip (ROC) electrically connected by bump-bonds to a pixel silicon sensor. The sensor matrix will be provided on wafers, while the ROCs are only available as single dies. *The company should then have a proven track record with hybridization process among sensors and single die readout chips.*

In this section the device technical specifications are detailed.

2.1. Sensor description

The pixel devices are fabricated with single side process on 6-inch diameter silicon-silicon Directs Wafer Bonded build by a high resistivity n-type wafer, in which the pixel unit cell are processed, supported by a low resistivity support wafer, (Figure 3). The support wafer is needed since the sensor is surrounded by trenches filled with poly-Si extending through all the active thickness. The support wafer is 250  $\mu\text{m}$  thick while the sensor wafer is 450  $\mu\text{m}$  thick.

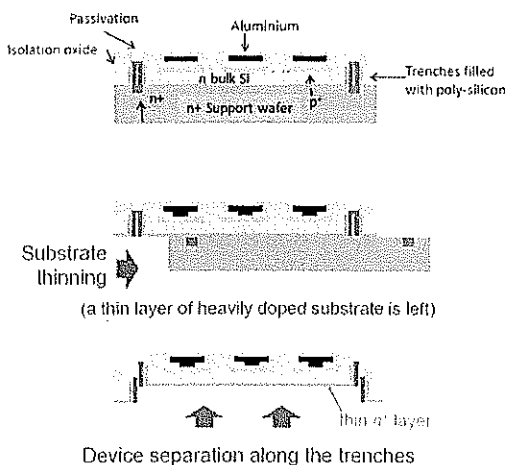


Figure 3: Cross section of active edge sensor wafer

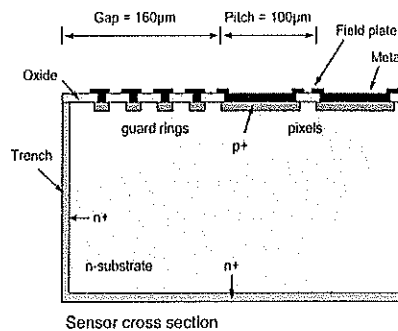


Figure 4: Matrix sensor cross section

The sensor to be used for the assembly is a 32x32 p+ on n active edge pixel matrix, with 110  $\mu\text{m}$  x 110  $\mu\text{m}$  pixel pitch, processed with planar technology. The matrix is surrounded by four p+ implanted guard rings and by the trenches, as shown in Figure 4 and 5. The external dimension of the sensor chip are 3.815 mm x 3.815 mm.

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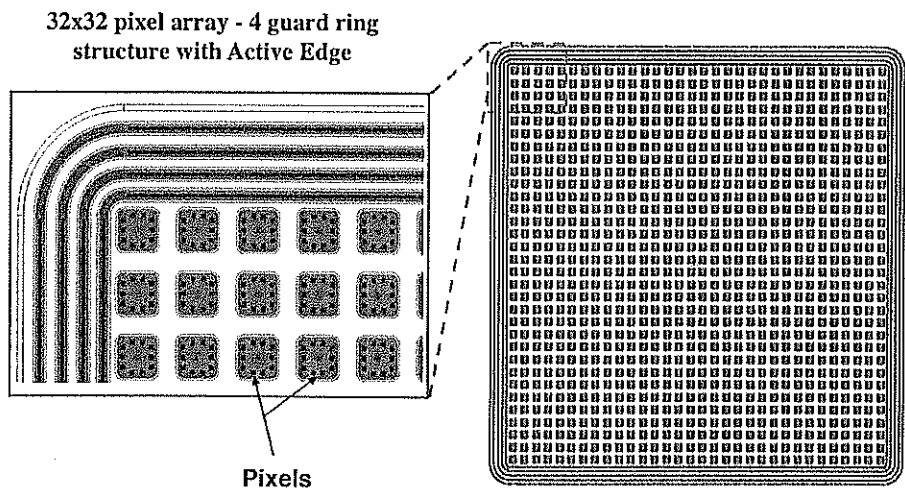


Figure 5: 32x32 pixel array

The layout of the full 6-inch wafer, shown in Figure 6, includes several different pixel arrays and test structures. Each wafer hosts 18 sensors of the type be used for the assembly, localized in region B18.

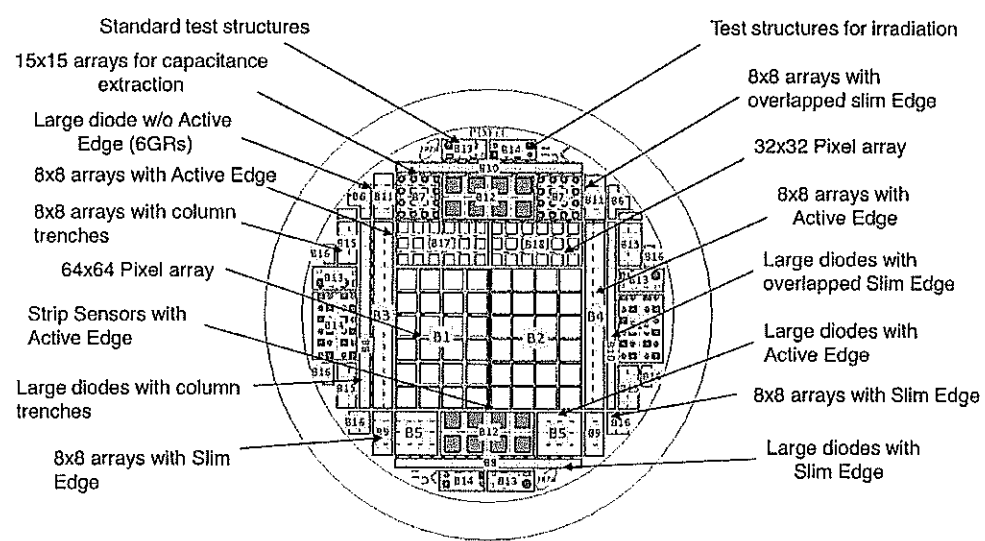


Figure 6: PixFEL wafer layout

The INFN will provide the GDS file of the sensor's layout needed to design the mask for Under Bump Metal deposition (UBM) on solder pads and alignment mark structures on the sensors. Three wafers (2+ 1 spare) will be supplied by the INFN and a map of the sensors to be used will be also provided.

2.2. Thinning of the Pixel Sensors wafers & sensor matrix separation

After the process steps needed for solderable pad deposition on the sensor matrix, and before the connection to the ROC, the backside 250µm-support wafer



needs to be removed. The wafer will be thinned, by grinding, to about 450  $\mu\text{m}$ , according to INFN prescription for the final thickness. After thinning the single active edge 32x32 pixel matrix need to be separated (Figure 3), inspected and stored into carriers (GelPack) before further processing steps.

*The vendor has to take precautions, ESD and mechanical, to protect the wafer and the solder pads against any damage during the thinning process (chipping, cracking, or shattering). All sensor wafer remnants after cutting should be sent back to INFN-Pisa with their individual tracking information, including wafer number and position in the wafer.*

### 2.3. ROC description

The PixFel ROC (PFM2) chip is a readout integrated circuit, consisting of 32x32 square cells. It has been designed in a TSMC 65 nm CMOS technology and is currently under test. The die covers an area of 4.324x3.830  $\text{mm}^2$  (including seal ring).

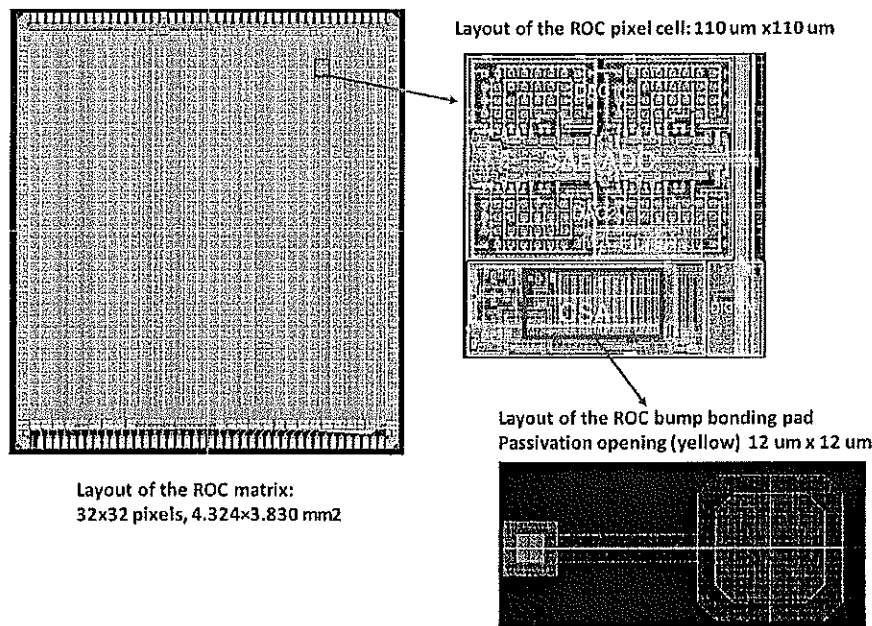


Figure 7: PFM2 ROC layout

The pixel cell covers an area of 110x110  $\mu\text{m}^2$ . The analog front-end of each pixel includes a Charge Sensitive Amplifier (CSA), a time variant filter and an Analog-to-Digital Converter.

The layout view of the chip is shown in Figure 7, where is also visible the detail of a single pixel cell, and the pad designed for the bump bonding with the sensor matrix. The passivation bump opening is 12  $\mu\text{m}$  x 12  $\mu\text{m}$  and passivation thickness is approximately 1  $\mu\text{m}$ .

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Beside the 32×32 matrix of pixels, other peripheral blocks are included in the chip. Moreover, two rows of wire bonding pads are distributed on the top and bottom side of the chip. *These wire bonding pads should not be affected by the hybridization processing.*

Since the chips have been produced in MPW they are available only as single dies and they should be embedded in a ceramic carrier wafer for the hybridization process. *The company should then have a proven track record in hybridization process among sensors and single die ROC chips.*

*The vendor has to take precautions, ESD and mechanical, to protect the ROCs against any damage during the process (chipping, cracking, or shattering)*

The INFN will provide the GDS file of the ROC's layout, needed to design the mask for bumps/UBM and alignment mark structures for the carrier wafer of the ROC chip.

#### 2.4. Process steps for single chip Assembly Procedure

The main process steps for the hybridization process of the single chip device are the following:

1. Design and mask preparation:
  - Preparation of gds2 bumping mask for single ROC chip carrier wafer (bump structures, alignment marks)
  - Preparation of gds2 UBM mask for sensor wafer (UBM pad structures, alignment marks)
  - 5" mask preparation for carrier wafer
  - 7" mask preparation for sensor wafer
2. Wafer and chip process:
  - Sensor wafer:
    - UBM deposition on sensor wafer
    - Backside carrier wafer removal (grinding/polishing, stop at pre-defined thickness)
    - Sensor chip separation and sorting
  - Readout chips:
    - Measurement of the X-Y dimensions of the ROC chips
    - Preparation of carrier wafer and chip attach
    - Solder bumping of readout chip
    - Demounting from carrier wafer (dicing)
    - Cleaning
3. Flip chip assembly:
  - Pick and place of readout chip onto sensor chip
  - Reflow soldering
  - x-ray inspection and documentation
  - shipment to INFN

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## 2.5. Bump Deposition and Flip-Chip specifications

The primary requirement for deposition of bumps (and/or UBM) on sensor and ROCs is to meet the fine pitch specification with high yield, which will allow the subsequent flip-chip assembly of the chips to the sensor with high yield of low electrical resistance connections. Specific requirements are:

1. Ability of the company to perform hybridization process among sensors and single die ROC with high yield
2. Alignment accuracy of flip-chip process better than 3  $\mu\text{m}$
3. Bump height after flip-chip assembly between 15 and 40  $\mu\text{m}$
4. Bump uniformity better or equal to 2  $\mu\text{m}$
5. Ability to supply complete information about x-ray inspection of the assembly after flip-chip process, needed to access the quality of the device.
6. Bump material composition must be specified by the vendor and approved by INFN. Same process for UBM, used to match the bump material and provide high yield during flip-chip assembly, long-term high quality contacts and avoid migration of bump material inside the wafer.
7. The process temperature profile must be specified
8. Flux less process should be used
9. Electrostatic discharge protection required during wafer handling and flip-chip assembly
10. Additional processing on the assembled device (wire bonding, gluing and mounting) will be necessary after hybridization. The bump deposition and flip-chip processing must be compatible with these additional assembly steps.
11. The wire bonding pads should be left clean by the process to ensure an easy and safe wire bonding with automatic equipment.
12. *The vendor has to take precautions, ESD and mechanical, to protect the sensors and ROC chips against any damage during the process (chipping, cracking, or damaged wire bonding pads)*

## 2.6. Material provided by INFN

- Sensor wafer:
  - 32x32 pixels silicon sensors with 110 $\mu\text{m}$  pitch on 6" wafers (2 +1 spare wafers);
  - Sensor wafer 450 $\mu\text{m}$  active thickness and are bonded to a 250 $\mu\text{m}$  support wafer
  - Sensors have an active edge with trenches extending through all the active thickness
  - The support wafer needs to be removed after processing
  - Gds2 layout file of top metal and passivation layer
- Readout Chip:
  - 10x ROICs with an area around 4 mm x 4 mm, available as singulated dies (number of final assemblies 10 + 2 spares);
  - Gds2 layout file of top metal and passivation layer (single readout chip)

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2.7. Material to be process by the vendor

- Design and produce 7 inches glass mask for UBM and alignment mark structures for the sensor wafer.
- Design and produce 5 inches glass mask for bumps/UBM and alignment mark structures for the carrier wafer of the ROC chip.
- Process 2 (+1) pixel sensor wafers as described in section 2.4
- Process 10 (+2) ROC chips as described in section 2.4
- Flip chip assembly of 10 (+ 2) single chip modules as described in section 2.4

2.8. Other details to be included in the bid

The vendor should provide INFN-Pisa with detailed information such the temperature under which the bumping process, including UBM deposition, will be carried out and its duration in time, the UBM thickness and metal type that will be used. If a subcontractor will be used in any phase of the work this should be clearly indicated in the bid, including the names of the sub-contractor(s).

2.9. Shipping and packaging

The vendor is going to deliver assembled device to INFN-Pisa.

The vendor should consult INFN-Pisa about the packaging of the parts before delivery.

3 Delivery and verification

3.1 Quality control during production

During the process of each device data is recorded in a vendor's lot tracking system about critical feature: x-ray inspection data, dimensions, thickness, bump heights etc. Tracking of ROC die bonded to device will be recorded by the vendor. All documents should be made available in electronic format upon agreement between INFN-Pisa and the vendor.

3.2 Delivery Time

Kick-off of the project is foreseen after contract is issued and material is delivered to the company.

The full assembly process should last 5 months.

The sensor - ROC assembly should be delivered to the INFN-Pisa.

3.3 Verification and certification

Within 1 month from delivery, the assemblies will be subject to a verification and certification by INFN personnel, who will test the system against the stated specifications. In general we will NOT ACCEPT bump bonded modules with one of the conditions listed below :

- Chipped edges
- Broken/cracked chips or sensor
- Unusable wire bonding pads

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Only the positive verification and certification will authorize the full contract payment by INFN.

#### 4 Minimal requirements to participate to the bid

Vendors can participate to the bid only if they can supply:

- *a proved ability to perform hybridization process among sensors and single die ROC with high yield following the specification detailed in Sec. 2.5*

#### 5 Bid evaluation criteria

The quotation will be evaluated on the basis of a figure of merit (FM) that combines the production time and the cost as described below.

##### 5.1 Rules for quotation evaluation and contract awarding

The quotation figure of merit  $FM(q)$  is calculated combining a number  $N$  of criteria according to the following formula:

$$FM(q) = \sum_{i=1}^N W_i V_i(q)$$

where:

- $W_i$  are the weights assigned to each criterion, with a total of  $\sum_i W_i = 100$ ;
- $V_i(q)$  are the calculated or evaluated coefficients for each criterion for the quotation  $q$  with  $0 \leq V_i(q) \leq 1$

Two types of criterion calculation are possible: qualitative and quantitative.

We define the following criteria:

Criterion	Description	Type	Weight
C.1	Delivery time	Quantitative	20
C.2	Cost	Quantitative	80

##### C.1 Delivery time

The delivery time value  $A(q)$  of each quotation is calculated as the percent reduction with respect to the base tender delivery requirement. The maximum quotation value  $A_{MAX}$  is then calculated and the individual coefficients calculated as follows:

$$V_3(q) = A(q)/A_{MAX}$$

##### C.2 Cost

The cost coefficient calculation proceeds as follows. The value of each quotation  $A(q)$  is calculated as the percent reduction with respect to the base tender cost, so that a quotation with lower cost has a higher value. The maximum and

average quotation values are then computed,  $A_{MAX}$  and  $A_{AVG}$ , and the individual coefficients calculated as follows:

If $A(q) \leq A_{AVG}$	$V_2(q) = XA(q)/A_{AVG}$
If $A(q) > A_{AVG}$	$V_2(q) = X + (1 - X)(A(q) - A_{AVG})/(A_{MAX} - A_{AVG})$

with  $X = 0.9$ .

#### 5.2 Option to purchase additional assemblies

INFN reserves the right to order additional modules, at the same unit prices and conditions as stated in the vendor bid, provided that the purchase option for additional modules is taken up by INFN not later than 2 months after the contract award. The cost of additional modules will not exceed 30% of the initial tender cost.

*RN Rec.*

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## ***Lotto B: Capitolato Tecnico*** **Lotto B: Technical Specifications**

**CMS Silicon Pixel R&D for Phase II**

**Chapters:**

0. Introduction
1. Batch-1 Device technical details
2. Batch-2 Device technical details
3. Single Chip assembly
4. Processing Schedule and Quality Assurance
5. Acceptance Criteria

R2D

**0. Introduction**

The Compact Muon Solenoid (CMS), experiment at the Large Hadron Collider (LHC) at CERN, planned the upgrade of the silicon pixel detector for the Phase II. This upgrade intends to replace the current pixel tracker with a new high efficiency and low mass detector. The conceptual layout is under study and the goal of the R&D in this proposal is to design and qualify the best performing and radiation tolerant pixel detector for Phase II upgrade.

In this proposal we are going to discuss the production of two lots of pixel devices. First lot (**Batch-1**) foresees the production of fully functional single ROC chip devices, while second lot (**Batch-2**) plan the production of dummy devices designed to study the bump bonding technology for high density of bumps.

The deliverables for this bid will be thinned, diced and single-chip assembled units that pass the acceptance criteria, the test results, and the process details, all as specified in following chapters.

In the following:

- 1) **batch-1** or **batch-2** identify the name of lots to be assembled. Details will be discussed in the following pages.
- 2) **INFN-Pisa** identifies the laboratory in charge of this R&D proposal.

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# 1. Batch-1: device technical details

## 1.1. Overview

This document contains the technical specification for the upgrade of the CMS pixel detector for Phase II and focuses on the silicon pixel device hybridization.

As non-exhaustive example we are showing here the basic unit of a prototypes to be produced by this R&D project. It consists of a readout chips (ROC) electrically connected by bump-bonds to a pixel silicon sensor. In the current prototype design each ROC has 52 columns  $\times$  80 rows and the unit size of a pixel sensor is  $150\mu\text{m} \times 100\mu\text{m}$ . The picture of the current pixel device is shown in Figure 1a with a few implant details shown in the Figure 1b. The project will deal also with different devices having larger number of columns and rows with modified pixel geometry and pitch.

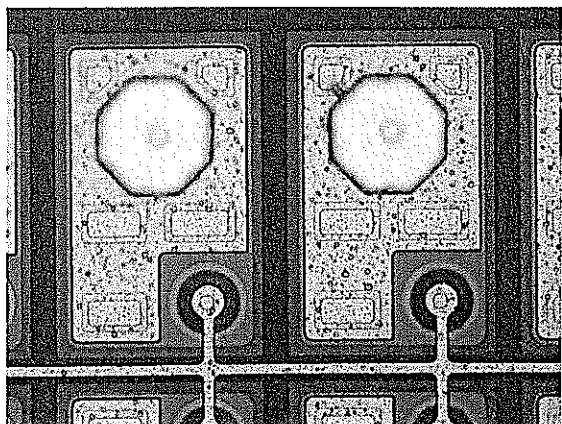


Figure 1a: Close view of  $150\mu\text{m} \times 100\mu\text{m}$  pixel

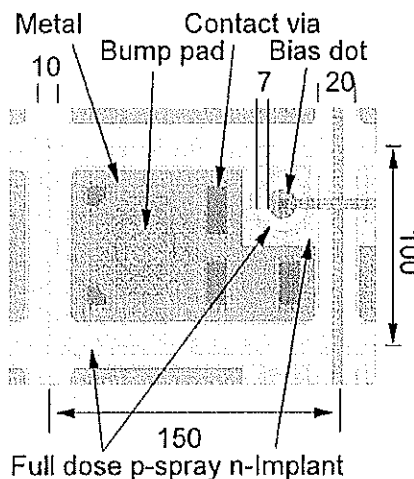


Figure 1b: Detail of the Pixel Unit Cell for a of  $150\mu\text{m} \times 100\mu\text{m}$  pixel. All distances are in  $\mu\text{m}$ .

The R&D discussed in this document plan to the optimization of the pixel unit design, following the qualification of new prototypes having the following main features:

- smaller pixel pitch, compared to current design;
- thinner active and full thickness, compared to standard of  $300\mu\text{m}$  in use;
- higher electrical interconnection density;
- improved radiation tolerance;

as specified in the following for **batch-1** and **batch-2** lots.

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## 1.2. Batch-1 Wafer description

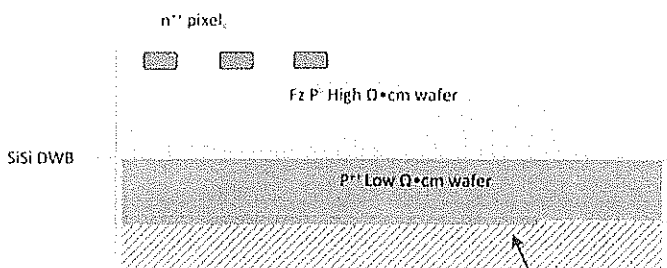
### 1.2.1. Pixel Sensor Wafer description

The pixel devices are fabricated with Single Sided process on 6-inch diameter wafers, silicon-silicon Direct Wafers Bonded (*DWB*) and SOI wafers, built on a low resistivity carrier wafer (p-type doped) as support of a high resistivity p-type FZ wafer as active layer in which the devices are processed. Support wafer is 500  $\mu\text{m}$  thick while two active wafer layer thicknesses are available: 100  $\mu\text{m}$  and 130  $\mu\text{m}$ .

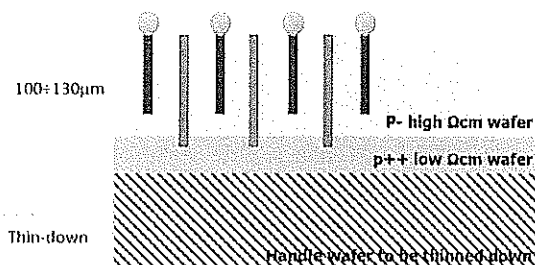
Wafers to be used in this project are processed with two different technologies:

- Planar pixels with junction build as layer on the surface by planar implant doping (*design-A*), see Figure 2a. This design will implement also Active/Slim edge as detailed in the next paragraph;
- 3D columnar pixel, having junction made by cylindrical doped columns, build by DRIE technology through the active thickness (*design-B*), see Figure 2b.

As shown in the figures handle wafer on the deliverables will be thinned down and eventually backside after thinning will be covered by metal contact layer.



2a: Design-A cross section of SiSi DWB wafer. Metal contact in the thinned backside is shown. Sketch view not in scale



2b: Design-B cross section of SiSi DWB wafer. Columnar implantation are shown: red are  $n^+$  doped (Junction), blue column  $p^+$  doped (Ohmic). Sketch view not in scale.

For both Design-A and Design-B sensor wafers will pass a QA procedure prior delivery to the vendor for hybridization, and a Known Good Die (KGD) map will be provided together with the wafers.

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### 1.2.2. Design-A Layout details

Design-A wafer layout is shown in Figure 3. The GDS file will be made available for mask design. Layout includes different pixel devices to be used in this project. Devices are grouped as underlined in the figure. The name is inherited by the corresponding ROC to be used in the hybridization process. For this project devices assembled with PSI type ROC chips will be used. The devices naming convention and details for the pitch (units are in  $\mu\text{m}$ ) are shown in the table 1.

PSI46dig	FCP130	RD53A	FE-14	R45	CLIC-PIX
			single & double	new PSI test roc	
100 x 150 std.	30 x 100	50x50	50 x 250 std.	50x50	50x50
50 x 50 adapt.		25 x 100		25 x 100	
25 x 100 adapt.					

Table 1: Names and pixel pitch details (in  $\mu\text{m}$ ) of devices implemented in Design-A

In the table the specification "std." means standard devices with pixel pitch similar to ROC chip; "adapt." identify devices with smaller pixel pitch adapted to the larger ROC chip pitch.

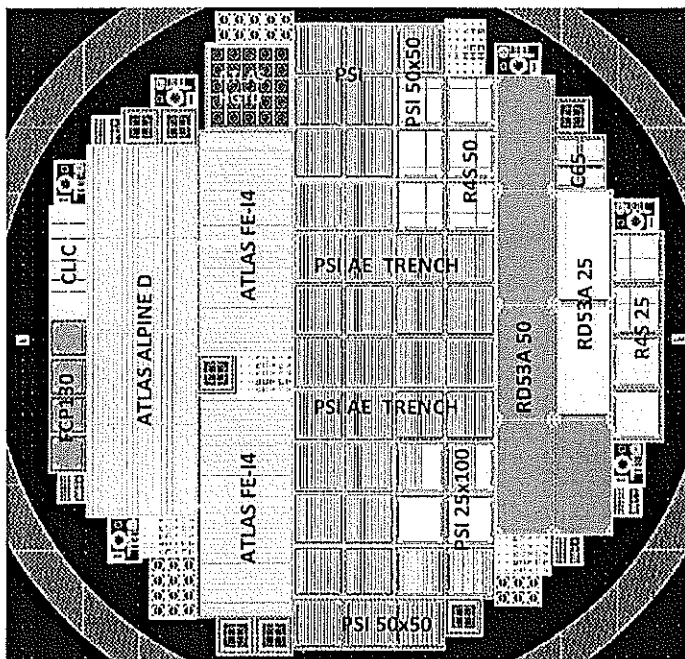


Figure 3: Layout of the Design-A wafer

In order to spot challenges for the hybridization steps a few layout details are listed in the following.

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Detail of a typical device in the periphery region is shown in Figure 4. It can be seen the corner of a device with dashed "staggered trench" and dicing lines. Cross section showing the geometry of a typical "trench" is shown in Figure 5: implant is built in depth through the active devices down to the carrier wafer. In order to exploit the performance of the trench design a second set of dicing lines are drawn, Optional dicing lines, designed nearby the trench structure (Figure 4).

In addition to the pixel devices the wafer includes, for the two layouts, test structures, diodes, gate-controlled diodes, MOS capacitors, and fiducial markers.

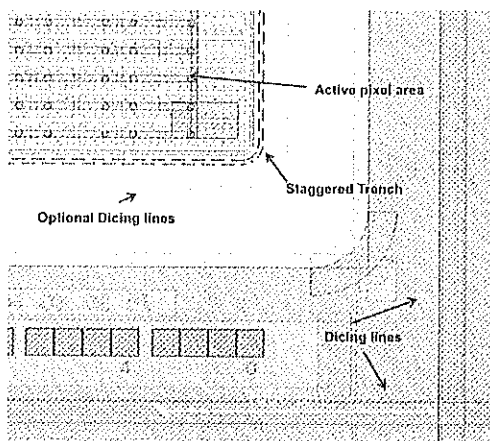


Figure 4: Corner of a Design-A device. Dicing Lines (path width 85  $\mu\text{m}$ ) and Trench implant can be seen.

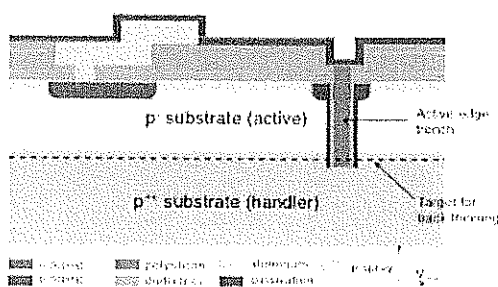


Figure 5: Cross section of a periphery trench implant, sketch view not in scale.

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1.1.1. Design-B Layout details

Design-B wafer layout is shown in Figure 6. The GDS file will be made available for mask design. Layout includes pixel devices to be used in this project. Devices are grouped as underlined in the figure. The name is inherited by the corresponding ROC to be used in the hybridization process. For this project devices assembled with PSI type ROC chips will be used. The devices naming convention and details for the pitch (units are in  $\mu\text{m}$ ) are shown in the table 2.

FE-14 (ATLAS)	FE-13 (ATLAS)	PSI46dig (CMS)	FCP	RD53
50 x 250 (2E) std	50 x 50 (1E)	100 x 150 (2E and 3E) std.	30 x 100 (1E)	50x50 (1E)
50x50 (1E)	25 x 100 (1E and 2E)	50x50 (1Eand2E)		25 x 100 (1E)
25x100 (1Eand2E)		50x100,100x100 (2E+4E)		25 x 100 (2E)
25 x 500 (1E)		50x100,100x150 (2E+6E)		
		25 x 100 (1E and 2E)		

Table 2: Names and pixel pitch details (in  $\mu\text{m}$ ) of devices implemented in Design-B

In the table specification "1E or 2E etc." means devices processed with Pixel Unit CEL (PUC) made by 1 or more columnar cells. As before "std." means PUC with pitch similar to the corresponding ROC chip.

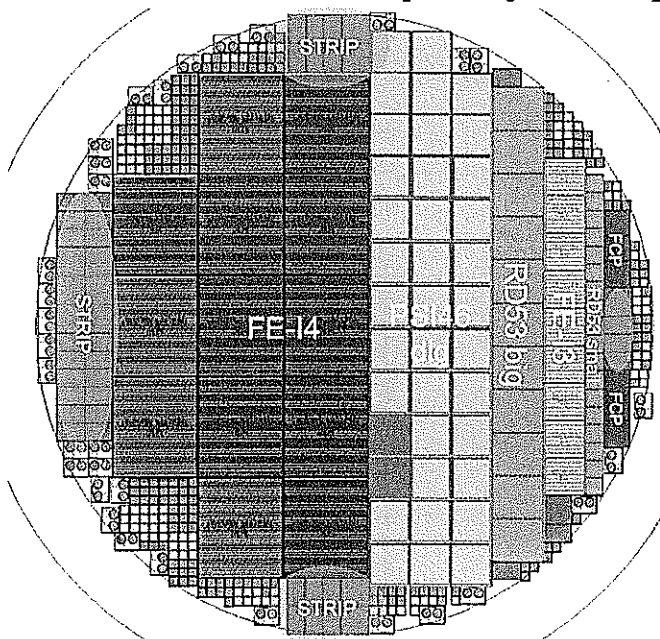


Figure 6: Design-B wafer Layout

In order to spot challenges for the hybridization steps a few layout details are listed in the following.

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Detail of a typical device in the periphery region is shown in Figure 7. It can be seen the corner of a 3D device with dicing lines, columnar periphery termination and the structure numbering.

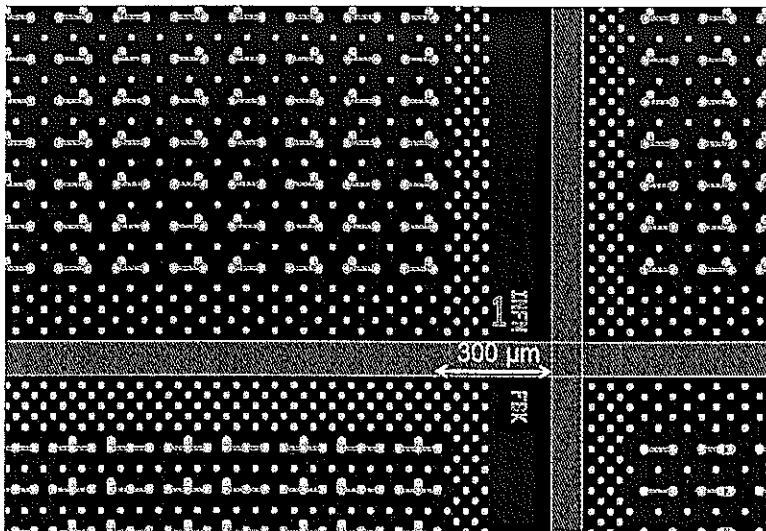


Figure 7: Corner of a 3D device (id n.1) included in Design-B. Dicing path width is 80  $\mu\text{m}$ .

A few details on column geometry and positioning of the bumps are discussed here. The layout foresees to have pixel devices in which bumps are to be positioned on specific pads connected by metal line to junction column implant and pixel devices where instead the bumps should stay on top of the column. Each column is filled by doped poly-silicon and covered by metal contact.

The bump dimension should be tuned according to the column geometry discussed in the following. Details are visible in figure 9 for a device with basic 3D cell  $50 \times 50 \mu\text{m}^2$ , two different arrangements are shown (9a(1E) and 9b (2E)). Bumps are not on top of the column. For a device  $25 \times 100 \mu\text{m}^2$  cell is shown in figure 10 for the configuration 2E.

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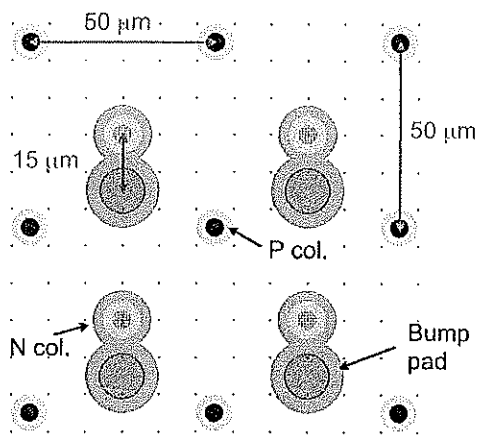


Figure 9a: 3D cell for a device 50 μm x 50 μm

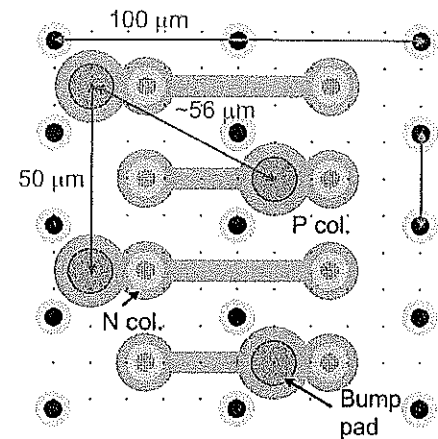


Figure 9b: 3D cell for a device 50 μm x 50 μm

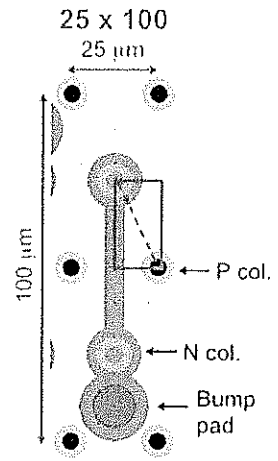


Figure 10: 3D cell for a device 25 μm x 100 μm

In addition to the pixel devices the wafer contains, for the two layouts, test structures, diodes, gate-controlled diodes, MOS capacitors, and fiducial markers.

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**1.2. Pixel Wafer thinning for Batch-1**

The Pixel sensor wafers thick 600-630  $\mu\text{m}$  have to be thinned according to INFN prescription and under agreement with company. We underline here, as example, that the smaller thickness we have achieved today on Silicon DWB wafers is  $180 \mu\text{m} \pm 5\mu\text{m}$ , with TTV smaller than  $5\mu\text{m}$ , very small roughness and stress release before the flip-chip assembly process.

Tuning of wafer thinning has to be considered for both design-A and design-B; the trench or 3D column implant near the devices periphery can make fragile the full wafer and this must be taken into account. Accidental breaking of no more than one wafer it is an acceptable risk.

The vendor has to take precautions, ESD and mechanical, in order to protect the wafer, the PUC and UBM from any damage during the thinning process: the wafers have to be suitably protected against any damage to the wafer (chipping, cracking, or shattering) and on bumps and other exposed metal layer structures.

**1.3. ROC Wafer Description**

Batch-1 devices (both design-A and design-B) will be connected with bump bonding to the readout chips (ROC) processed in 8-inch in diameter and with standard thickness (750-825  $\mu\text{m}$ ).

Each readout chip is processed by standard CMOS technology: 0.25  $\mu\text{m}$  technology for PSI46dig and PROC600.

Each ROC PSI46dig measures about 10.2 mm x 7.9 mm. There are 62 four-ROCs blocks ("reticle") on each wafer as shown in Figure 11 for a total of 248 chips, with  $100 \mu\text{m} \times 150 \mu\text{m}$  pitch. Similar layout and geometrical features are valid for the other PSI ROC wafer to be used in this project PROC600.

For PROC600 each reticle hosts 3 ROC chips equivalent to PSI46dig plus one ROC4sens with pitch 50  $\mu\text{m}$  in both directions.

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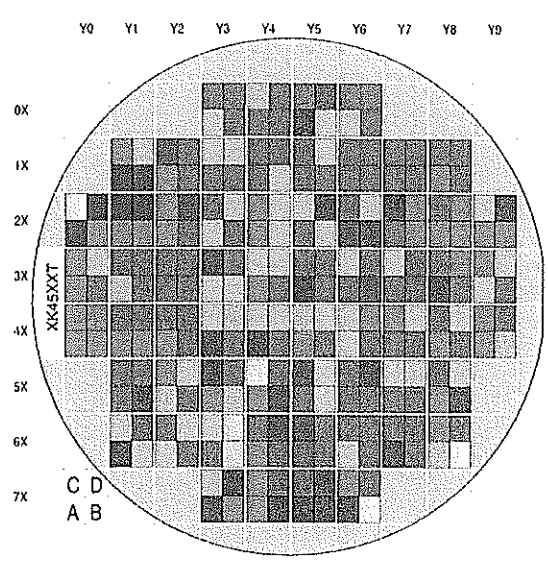


Figure 11: Floor plan of PSI46dig ROC wafer. ROCs are organized in blocks of four chips (according to lithography reticle), 248 in total.

The chips will be tested on the wafer before the delivery to hybridization vendor and a Known Good Die (KGD) map will be provided together with the wafers.

**1.3.1. ROC Wafer thinning**

The ROC wafers, PSI46dig and PROC600, have to be thinned to a standard thickness usually around  $175\mu\text{m} \pm 5\mu\text{m}$ , with TTV smaller than  $5\mu\text{m}$ , very small roughness and stress release before the flip-chip assembly process. The vendor has to take precautions, ESD and mechanical, to protect the wafer and the bumps from any damage during the thinning process. The wafers have to be suitably protected against any damage to the wafer (chipping, cracking, or shattering), the bumps, and the wire bond pads.

All wafer remnants after cutting should be sent back to INFN-Pisa with their individual tracking information, including wafer number.

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#### 1.4. Dicing specification for Pixel sensors devices and ROC chip

The pixel wafers must be diced in individual single Pixel sensors and ROC wafers must be diced in individual ROC chips. All guard rings or most external implants should be at least 30 microns away from the kerf edge. The dicing tolerance is  $\pm 20$  microns. The kerf width should be less than  $50\mu\text{m}$ . Dicing should be done with a saw compatible with these specifications. The grit/concentration used should agree with the industrial standard for dicing silicon. De-ionized water should be used during dicing.

All wafer remnants after cutting should be sent back to INFN-Pisa with their individual tracking information, including wafer number.

## 2. Batch-2: device technical details

### 2.1. Overview

The goal of this processing is the study of Bump Bonding with high interconnection density. Today we have experience with prototypes assembled with about  $5000$  bumps/cm<sup>2</sup>. Future pixel detectors will be hybridized with an interconnection density  $\sim 6-10$  times higher. Realistic design for such detectors foresees a unit sensitive area of  $\sim 4$  cm<sup>2</sup>, and the detector unit is built by hybridization of one ROC and one pixel sensor.

For this study we plan to use pixel devices and ROC not fully functional as detectors (dummy devices), built by metal layer deposition on virgin silicon wafers. In order to test consistently the bump bonding process at vendor the plan foresees the use of 8-inch or 6-inch wafers for ROC and 6-inch wafer for sensor dummy devices.

The silicon material has to be thinned and diced (for specification see details described for batch-1) in order to evaluate the final assembly performance after the full processing steps and in standard conditions.

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## 2.2. Batch-2 Wafer description

### 2.2.1. Pixel Sensor and ROC Wafer description

The basic functionalities to be studied with a target detector unit of  $-4 \text{ cm}^2$  area and thinned thickness, are the following:

- Count of bump defects for unit detector
- Measurement of interconnection resistance of bumps, with 4 points method.

The proposal consists of a design of a set of test structures build by arrays of bump bonds, in which an optimized fraction of them have been connected, in one direction, by metal lines to form daisy chains, and the rest are short-circuited, in the same direction, to connect the daisy chains to the external pad connections.

The test structure is actually a whole assembly, and therefore, composed of two sides for the flip chip process. One of them is the 'chip' side ("Dummy ROC" c-side processed on 8 inch wafer or 6 inch wafer) with the metal pattern to make one half of the daisy chains, plus the corresponding fan-out to the test pads for automatic testing. The 'detector' side ("Dummy Sensors" d-side processed on 8 inch wafer or on 6 inch wafer) contains only the corresponding metal pattern to match with the c-side forming the daisy chain structure. Wafer size selection is left to vendor choice.

The daisy chains are uniformly distributed in the test structure in order to cover the whole assembly area of about  $4 \text{ cm}^2$ .

In addition, two ground busses, with all their bump bonds short-circuited, cross the assembly in perpendicular directions roughly at the middle of the assembly in order to facilitate the connection of the daisy chains to ground for the testing.

The test structure is therefore, a full assembly made of a series of long bump bond daisy chains that are evenly distributed across the whole area of the assembly.

Each daisy chain contains a number  $N$  of bump bonds tuned considering the quality test significance. Each chain is connected in a way that if any of them fails, the whole chain is electrically open. Figure 12 shows a schematic cross-section of a daisy chain in the assembly.

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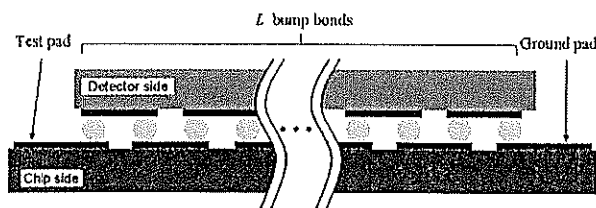


Figure 12: cross section of a device implemented in Batch-2 Layout

The chains are then connected to test pads prepared for automated measurements with a probe station.

The layout will be discussed between vendor and INFN-Pisa: INFN-Pisa will provide basic cell design (drawing) for connections that will be modified and implemented by the vendor in a gds file for masks preparation.

This study should consider, for a "typical future detector", a density of 160000-320000 ( $50\mu \times 50\mu - 100\mu \times 25\mu$  pitch) bumps on a  $4 \text{ cm}^2$  device.

The goal consists in verifying the feasibility of the hybridization step for a "typical future detector".

In order to face realistic processing issues we target also on thinning dummy pixel wafer and dummy ROC wafer down to about  $200 \mu\text{m}$ . The actual limit will be discussed with the vendor.

As comparison it is foreseen the design of standard devices with bumps density as commonly used today too.

The wafers layout will be discussed and agreed between INFN-Pisa and vendor.

Vendor should be capable to provide the full process:

- GDS layout design
- Mask preparation
- Wafer procurement
- Metal layer deposition steps
- Oxidization step and opening on passivation
- Any extra layer deposition deemed necessary by the vendor for the bump bonding technology selected and agreed with INFN-Pisa
- All steps as discussed previously for hybridization of batch-1

The number of wafers processed is planned to be small: for "ROC dummy" wafers 1-2 ROC 8-inch wafers or 2-3 6-inch wafers, for "Sensor dummy" 2-3 6-inch or 8-inch wafers.

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Bump geometry details will be discussed and agreed with INFN-Pisa in order to maximize yield and performance.

### 3. Single Chip assembly

#### 3.1. General consideration on Single Chip Assembly Procedure

The assembly of the modules has the following steps:

- 1) Production of the masks for Bumps and UBM deposition according to the GDS files provided for batch-1 by INFN-Pisa, provided by the vendor for batch-2. This is done preliminary to the production.
- 2) Bump deposition and/or UBM deposition on ROC and or on Pixel sensor wafers.  
The bump center-to-center spacing is from 100  $\mu\text{m}$  down to 50  $\mu\text{m}$  for batch-1, 50  $\mu\text{m}$  for batch-2, in the smallest dimension. The bump pattern is replicated in columns and rows on each of the ROCs and matches the same pattern on the pixel sensor.
- 3) Photoresist protection of the bumps, that has to be done before thinning and dicing.
- 4) Thinning of the ROC and sensor wafers as specified above. Thinning must include grinding defect removal and surface polishing.
- 5) Dicing/cutting of the ROC wafers and Pixel sensor wafers.
- 6) Test of the basic ROC functionality after thinning and dicing on tape. The feasibility and the procedure of this test will be discussed and agreed between vendor and INFN-Pisa.
- 7) Flip-chip assembly of the ROCs to pixel sensor.
- 8) Visual inspection and recording of inspection data at each step.
- 9) Each ROC after Flip Chip Bump Bonding should be X-ray inspected and recorded picture should be made available.
- 10) Prototypes delivery should be done with appropriate packaging (ESD safe). The packaging should be discussed with INFN-Pisa prior to shipment.

Other tests to be specified by the vendor and agreed upon by INFN-Pisa can also be performed for QA purposes.

The vendor should provide data in electronic/numeric format: in order to reveal the bump, interconnection or wafer characteristics, pairing of ROCs on Large Pixel sensors, possible ROC reworking, etc. The vendor should

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inform INFN-Pisa about possible technical problems or any other delays as early as possible.

### 3.1.1. Bump deposition and Flip-Chip specifications

The primary requirement for deposition of bumps (and/or UBM) on the sensor and ROC wafers is to meet the fine-pitch specification with high yield, which will allow the subsequent flip-chip assembly of the chips to the sensor with high yield of low electrical resistance connections. Details listed in the following refers to hybridization of Batch-1, specific chapter is dedicated to Batch-2.

Specific requirements are:

- 1) Bump material composition must be specified by the vendor and approved by INFN-Pisa. Same process for UBM, used to match the bump material and to provide high yield during flip-chip assembly, long-term high quality contacts and avoid migration of Bump material inside the wafer.
- 2) The process temperature profile must be specified with a maximum of 350 °C.
- 3) Flux less process should be used.
- 4) Center to center Bump pitch: 50  $\mu\text{m}$  minimum.
- 5) The bump diameter should be not larger than 40  $\mu\text{m}$ , for PROC600 to be optimized according to layout constraints.
- 6) Passivation opening for bump: according to point 5).
- 7) Alignment accuracy of flip-chip process: better than 3  $\mu\text{m}$
- 8) Bump height after flip-chip assembly: minimum 15  $\mu\text{m}$
- 9) Bump Uniformity:  $\leq 2 \mu\text{m}$  (wafer 8")
- 10) Electrostatic discharge protection required during wafer handling and flip-chip assembly.
- 11) Additional processing on the bare module (wire bonding, gluing and component mounting) will be necessary after the hybridization. The bump deposition and flip-chip processing must be compatible with these additional assembly steps.
- 12) The wire bonding pads should be left clean by the process to ensure an easy and safe wire bonding with automatic equipment. Wire bonding tests, on sample, will be made on test structures from the ROC wafers before and after bumping to verify that the pads have not been degraded during the processing.

12)

The following points constitute additional criteria for deliverables acceptance; reference values are listed in Chapter 3 (Acceptance Criteria):

- 13) Missing or merged bump defect rate, as determined by visual inspection on a wafer, and after flip-chip assembly as determined by X-ray inspection or other means should smaller than 2% per device unit.
- 14) The chips should adhere firmly to the sensor after mating, and should detach only if pull force larger than 0.2 g/bump (Indium bump material) or 1.5 g/bump (other bump materials).
- 15) The total leakage current of a sensor must not increase too much after the dicing process. In particular the device should be operational at least up to the depletion voltage before the hybridization step.

**3.1.2. Single Chip Assembly High density Bump Bonding project**

The single chip assembly for Batch-2 follows similar specification listed previously for Batch-1 with the exception of following points: 4), 5), 6), 8) and 15). Bump and UBM geometry (points 4), 5), 6) and 8)) should be optimized according to the device pitch. The point 15) is not applicable given that we are using dummy devices.

After approval of the vendor wafer Layout the proposal for bump, UBM geometry and material will be discussed and agreed with INFN-Pisa.

**3.2. Materials provided**

**3.2.1. By CMS**

For the Batch-1 production run, INFN-Pisa will provide to the vendor:

- 1) Up to 6 pixel silicon sensor wafers (DWB or SOI, 150 mm diameter).
- 2) Up to two silicon ROC wafers (200 mm diameter).
- 3) Files of the wafers layout in GDS format.
- 4) Conceptual drawing of Benzo-Cyclo-Butene (BCB) mask.
- 5) KGD map for each ROC wafers and KGD map showing the good pixel sensors on the sensor wafers based on our



tests. Only the good ROC dies and pixel sensors should be used in the assembly process.

For the Batch-2 production run, INFN-Pisa will provide to the vendor:

- 1) Conceptual sketch agreed with the vendor, of ROC and Sensor wafer Layout

**3.2.2. By Vendor**

For the Batch-2 production run, the vendor will provide

- 1) Dummy Pixel silicon sensor wafers, (6-inch or 8-inch).
- 2) Dummy silicon ROC wafers (6-inch or 8-inch).
- 3) Files of the wafers layout in GDS format.
- 4) KGD dies map after optical inspection of parts.

**3.3. Materials to be processed in this project**

Vendor bid should be issued accordingly to the following list:

**3.3.1. Batch-1 Design-A and B**

Pixel wafers:

- 1. Units to be processed: 2 Design-A + 2 Design-B. Appropriate mask should be designed and produced.
- 2. Back side metallization: a uniform metal layer should be sputtered in the backside after wafer thinning. No masking is required unless this is deemed necessary by the vendor.
- 3. Exclusively for Design-A: a Benzo-Cyclo-Butene (BCB) protection layer should be deposited on the wafer in order to protect devices from sparks. Appropriate mask should be designed and produced.

Quotation should detail the cost for "first wafer" processed for both designs, for the "second wafers" (and for eventual more wafers beyond this offer).

ROC wafers:

- 4. Units to be processed: one PROC600 wafer. Appropriate mask should be designed and produced
- 5. BCB protection layer should be deposited on the PROC600 wafer in order to protect devices from sparks. Appropriate mask should be designed and produced.

Quotation should detail the cost for "first wafer" processed (and for eventual more wafers beyond this offer).

Flip Chip Bump bonding:

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- 6. Devices Design-A: 28 units to be assembled
  - 7. Devices Design-B: 40 units to be assembled
- Design-A or Design-b: any extra minimal-size lot to be assembled (and for eventual more assemblies beyond this offer).

### 3.3.2. Batch-2

The following list is a proposal that can be discussed with vendor for points 1. and 2.

Pixel wafers:

- 1. Units to be processed: 2 equivalent wafers.  
Appropriate mask should be designed and produced

ROC wafer:

- 2. Units to be processed: 2 equivalent wafers.  
Appropriate mask should be designed and produced

Flip Chip Bump bonding:

- 3. Units to be assembled: 20 units to be assembled
- 4. Any extra minimal-size lot to be assembled (and for eventual more assemblies beyond this offer).

For Batch-1 and Batch-2 INFN-Pisa reserves the right to order additional Flip-chip at the same unit price and conditions as stated in the vendor bid, provided that the purchase option for additional modules does not imply processing of new wafers.

### 3.4. Other Details to be Included in the Vendor bid

The vendor should provide to INFN-Pisa detailed information such as the temperature under which the bumping process, including UBM deposition, will be carried out and its duration in time, the UBM thickness and metal type that will be used.

The vendor should inform INFN-Pisa of their dicing tolerance, preferably with illustrative photographs and/or statistical data, and whether they will do the dicing in-house or if this will be sub-contracted. If a sub-contractors will be used in any phase of the work this should be clearly indicated in the bid, including the names of the sub-contractor(s).

### 3.5. Shipping and Packaging

The vendor is going to deliver assembled pixel bare modules to the final destination CERN Route de Meyrin 385, 1217 Meyrin (CH) or CERN F01631 Preveessin CEDEX (Fr) site for EU vendors. The vendor should consult INFN-Pisa about the packaging of the parts before delivery.

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## 4. Processing Schedule and Quality Assurance

### 4.1. Introduction

This chapter covers the estimated timeline for wafer project and the quality assurance (QA) plan for the silicon pixel sensors Hybridization.

### 4.2. Timelines for Wafer Processing

Kick-off of the project is foreseen after contract is issued and material is delivered to the company.

The production can be scheduled in sub-lots regularly delivered by month basis, upon request of INFN and agreement with the vendor.

The **production kick-off** for each batch is defined by the arrival of the materials from INFN-Pisa and/or agreement between INFN-Pisa and vendor about mask designs.

The preliminary proposal for delivery follows:

- Batch 1 Design-A can be scheduled in 2 sub batches
  - First sub batch should be processed and delivered within 12 weeks from **production kick-off**
  - Production should last a maximum of **12 months**
- Batch 1 Design-B can be scheduled in 4 sub batches
  - First sub batch should be processed and delivered within 12 weeks from **production kick-off**
  - Production should last a maximum of **12 months**
- Batch 2 can be scheduled in 2 sub batches
  - First sub batch should be processed and delivered within 18 weeks from **production kick-off**
  - Batch 2 production should last a maximum of **12 months**.

Delivery of batches as scheduled will allow a better management of the production and eventual feedback to vendor if production issues are detected as explained in the following chapter.

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#### 4.3. Quality Assurance

In order to ensure consistent quality throughout the hybridization process, the following steps will be taken:

- A monthly status report will be submitted to INFN-Pisa to summarize the project status.
- During the processing of each device data is recorded in a vendor's lot tracking system about critical feature dimensions, film thicknesses, bump heights, etc. This data will be provided to INFN-Pisa during lot processing as part of the report, and any issues will be discussed.
- Tracking of ROC die bonded to device will be recorded on appropriate maps as provided by INFN-Pisa.
- All documents should be made available in electronic format upon agreement between INFN-Pisa and vendor.

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## 5. Acceptance Criteria

### 5.1. Overview

This chapter summarizes the **Acceptance Criteria** for the assembled parts and the **Evaluation Criteria** for the procurement.

Configuration and technical specification are detailed in the chapters 1 to 3 of the **Technical Specification** document.

The present devices assembled by the vendor will be injected in a chain of assembly steps that will assess the quality according to the number of pixel defect per device and the total current measured at operating voltage.

### 5.2. ACCEPTANCE CRITERIA

The goals of the Project are:

- to obtain the required number of adequately functioning assembled devices with the fewest defective interconnections and the least waste of ROCs and Sensors for the best price;
- to select a vendor that can meet our delivery schedule.

The present hybridization project will be monitored at level of devices upon reception at INFN-Pisa laboratory. In order to meet the condition for the majority of the devices to be classified as accepted, or category "A", we are using a set of acceptance criteria for the hybridization step listed in the following.

In this section we describe how we will determine that a vendor can produce modules with an acceptable yield and explain the **Figure of Merit** we will use to evaluate bids.

All inspections, mechanical and electrical tests described below will be performed by the **INFN-Pisa** upon reception.

Vendor should be able to meet the following requirements

#### The Requirements are:

**R.0** The vendor should setup a QA plan, to be supplied in the vendor bid. Specifically, the document should include:

- a. QA method to ensure lot-to-lot consistency.

- b. Description of X-ray and pull tests facilities and procedures.
  - c. Format of data to be provided to INFN-Pisa.
  - d. Method allowing INFN-Pisa to track the status of the processing.
  - e. Monthly status report document proposal.
- We will NOT ACCEPT vendor bid without QA plan as requested.

**R.1** The vendor should setup a production plan, to be supplied in the vendor bid. Specifically, the document should include the Production and delivery schedule.

In general, we will NOT ACCEPT vendor bid with production plan:

- a. Longer than 12 months.
- b. Having a production rate conflicting the one proposed in this document.

For item a. delays due to INFN-Pisa will not be accounted in the total time figure.

**R.2** In general, we will NOT ACCEPT Bump-Bonded modules with one of the conditions listed below:

- a. chipped edges;
- b. broken/cracked chips or sensor;
- c. unusable wire bonding pads.

For items a. and b., non-compliance is established by picture documented visual inspection. Most external implant in the periphery should be at least 30 microns away from the kerf edge. The dicing tolerance is  $\pm 20$  microns. The kerf width should be less than  $50\mu\text{m}$ . Dicing should be done with a saw compatible with these specifications. The grit/concentration used should agree with the industrial standard for dicing silicon. De-ionized water should be used during dicing.

For item c. the wire bonding pads should allow wire bonding with a standard automatic machine. Wire bonding tests, on samples, will be made on test structures from the ROC wafers before and after bumping to verify that the pads have not been degraded during the processing.

Furthermore, the following requirements must be met (all modules must satisfy all the requirements, except for "pull strength," criterion R.4 below):

**R.3** The mechanical tolerances listed in the Device specification chapter must be met:

- 1) Center to center Bump pitch:  $50\ \mu\text{m}$  minimum.

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- 2) The bump diameter should be not larger than 40  $\mu\text{m}$ .
- 3) Passivation opening for bump: according to point 2)
- 4) Alignment accuracy of flip-chip process: better than 3  $\mu\text{m}$
- 5) Bump height after flip-chip assembly: minimum 15  $\mu\text{m}$

**R.4** The pull strength of the ROC should be no less than 0.2 g/bump in case of Indium bumps and no less than 1.5 g/bump for other bump materials.

This will be determined by testing (at room temperature: 20°C) on a few parts, by sampling on good modules or on modules that failed one of the electrical tests.

**Following points (R.5-R.6) should be applied to batch-1 only.**

**R.5** The Pixel devices from the KGD maps meet a set of electrical specifications upon delivery. The same specifications must be met post hybridization. The total leakage current of a sensor must not increase too much after the dicing process. In particular the device should be operational at least up to the depletion voltage before the hybridization step. In case of non-compliance investigation must be undertaken together by INFN-Pisa and vendor in order to solve issues.

**R.6** The ROCs from the KGD maps meet a set of electrical specification upon delivery. The same specification must be met post hybridization. In particular:

**R.6.1** All ROCs on the bump-bonded module are functional (can be powered on and off, registers/DACs can be loaded, data can be readout). This test will be performed at room temperature.

**R.6.2** The number of bumps missing, bridged, or failing electrical tests at room temperature must be fewer than 100 on any ROC (~2.5%), in addition to the bad pixels already identified at delivery to the vendor. This test will be performed on devices after assembly.

In order to meet quality cuts applied in R.6 single ROC chip reworking can be performed:

**R.6.3** single chip reworking made by vendor should be notified to INFN-Pisa and documented.

**R.6.4** single chip reworking can be performed also upon INFN-Pisa request after QA test.

R.7 Modules failing the test criteria listed in this section will be rejected. The ratio between good Flip chipped modules produced and good sensors received define the yield, Y and the inefficiency (1-Y).

### 5.3. EVALUATION AND CONTRACT MONITORING

#### 5.3.1. Rules for Quotation analysis and Awarding of the contract.

The quotation will be evaluated according to qualitative and quantitative criteria. A total of 100 points score are available for the evaluation.

The qualitative criteria consists on the accomplishment of the requirements:

R.0, the score assigned is equal to 20 points. For this qualitative criterion each committee member will assign a coefficient indicating the level of compliance with the requested specifications, using as a guide the following scale:

The QA plan does not meets the requirements. Unaccettable	0
The QA plan is almost absent. Almost unacceptable.	0.1
The QA plan is very poorly presented.	0.2
The QA plan is poorly presented.	0.3
The QA plan does not present technical details, with few points missing. Unremarkable	0.4
The QA plan does not present technical details, with one point missing. Somewhat expected	0.5
The QA plan does not present technical details. Acceptable	0.6
The QA plan all points answered good	0.7
The QA plan all points with partial technical detail. Very good	0.8
The QA plan all points with 1 missing item detail. much better than expected	0.9
The QA plan is well discussed in requirements and technical details	1

The individual committee members coefficients are averaged to obtain the un-normalized committee coefficient for a specific criterion and a specific quotation. Finally, for each criterion, the un-normalized committee coefficients of the various quotations are divided by the maximum coefficient scored by any quotation for that criterion, obtaining the final coefficients, normalized to 1, as prescribed from "Linee Guida ANAC n. 2

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recanti: offerta economicamente più vantaggiosa approvate dal Consiglio di Autorità con Delibera n.1005 del 21 Settembre 2016"<sup>1</sup>

For the **quantitative** evaluation we have reserved 80 points score, and the quotation will be evaluated by providing a Figure of Merit, through a weighted sum of criteria and goals as detailed below.

The vendor with the highest figure of merit and who can meet the proposed schedule will be awarded of the contract.

The Figure of Merit is calculated by the following formula

$$FM = \sum_1^n (Max\ score)_i W_i V_i$$

where **Max score** is the value in points per criterion; the sum of all **Max scores** is equal to 100.  $W_i$  is the weight for the coefficient  $V_i$  assigned to each criterion.

Each  $V_i$  is evaluated by comparing the current offer with the "best" offer as explained in the following

We define the following criteria:

$V_1$  "cost of the project" (max score=60 points)

$V_2$  "delivery time" (max score=20 points)

**Definition of  $V_1$  cost of the project and  $W_1$**

Project Cost has the following evaluation: we consider  $C$  the percentage of reduction of the  $C_{OFF}$  current offered cost compared to the  $C_{INFN}$  foreseen cost  $C = (C_{INFN} - C_{OFF}) / C_{INFN}$ .

The  $V_1$  is defined as  $V_1 = C / C_{max}$  where  $C_{max}$  is the highest percentage of reduction offered.

The weighting factor  $W_1$  is equal to 1.

**Definition of  $V_2$  Delivery Time and  $W_2$**

Previous experience shows that the hybridization process request is compatible with a delivery time of  $T_n = 12$  months.

<sup>1</sup>The document (in Italian) is available for download at the following web address: [http://www.anticorruzione.it/portal/public/classic/AttivitaAutorita/AttiDellAutorita/\\_Atto?ca=6605](http://www.anticorruzione.it/portal/public/classic/AttivitaAutorita/AttiDellAutorita/_Atto?ca=6605)

Given  $T_c$  the current vendor quoted delivery time, we consider the reduction of the delivery time  $\Delta T_c = (12 - T_c)$ :  $R_c$  percentage of reduction of  $\Delta T_c$  compared to  $T_n$ .  
 The  $V_2$  is defined as  $V_2 = R_c / R_{max}$  where  $R_{max}$  is the highest percentage of reduction offered.

The weighting factor  $W_2$  is equal to 1.

**5.3.2. Quality Assurance in production**

We will monitor the quality of the assembly by measuring the Yield on the received modules. The Yield is evaluated on the bases of the delivery and INFN-Pisa will provide feedback within one week to the vendor on the results and help to solve problems.

**Contract Technical Clauses and breakdown of Penalties, intended as integration of the Contract Clauses document.**

In the event of non-performance or improper performance of the contract the vendor will be charged a penalty with criteria detailed in the following.

**TC0:** If the schedule slips by one month and if the production rate is not recovered within next month  
**Penalty is equal to 2% of the contract.**

**TC1:** If the production Yield should fall below 50% for a sub-lot delivered,  
**Penalty is the following: the vendor should produce more modules to reach at least 50% the sub-lot initial request without additional costs.**

**TC2:** Once agreed upon, any proposed change with respect to the approved Production and QA Plan during the Production Phase must be subject to prior approval by INFN-Pisa in writing.  
**In case of not observance the Penalty is equal to 2% of the contract.**





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## CONDIZIONI CONTRATTUALI

### 1. VALIDITA' OFFERTA:

Le offerte devono avere una validità non inferiore a 180 giorni.

### 2. GARANZIA DEFINITIVA:

L'esecutore del contratto è obbligato a costituire una garanzia definitiva secondo quanto previsto all'art. 103 del d.lgs. 50/2016, mediante cauzione o fideiussione bancaria o polizza assicurativa. L'importo della garanzia è ridotto nel suo importo in tutte le ipotesi previste dall'art. 93, comma 7, del d.lgs. 50/2016.

L'atto fideiussorio deve prevedere espressamente la rinuncia al beneficio della preventiva escussione del debitore principale; la rinuncia all'eccezione di cui all'art. 1957, comma 2, del Codice Civile, nonché l'operatività della garanzia medesima entro 15 giorni, a semplice richiesta scritta dell'INFN.

La cauzione è prestata a garanzia dell'adempimento di tutte le obbligazioni del contratto e del risarcimento dei danni derivanti dall'eventuale inadempimento delle obbligazioni stesse, nonché a garanzia del rimborso delle somme pagate in più all'esecutore rispetto alle risultanze della liquidazione finale, salva comunque la risarcibilità del maggior danno verso l'appaltatore e cessa di avere effetto solo alla data di emissione del certificato di collaudo provvisorio o del certificato di regolare esecuzione.

L'Impresa si impegna a tenere valida ed efficace la garanzia per tutta la durata del contratto e a reintegrarla ove l'INFN se ne sia avvalso, entro 10 (dieci) giorni dalla richiesta. In caso di mancato reintegro il contratto si intende risolto, salvo il risarcimento del danno.

### 3. PENALI:

In caso di mancato o inesatto adempimento delle prestazioni contrattuali sarà applicata una penale pari al 0,5% dell'importo contrattuale con un massimo del 5%.

La fissazione delle penali non preclude la risarcibilità di eventuali ulteriori danni o la risoluzione del contratto se l'ammontare delle penali raggiunge l'importo della garanzia definitiva.

### 4. TERMINI DI CONSEGNA:

La fornitura dovrà essere consegnata secondo i tempi e le modalità indicate nel Capitolato Tecnico.

### 5. SUBAPPALTO:

L'Impresa potrà subappaltare le prestazioni contrattuali dietro autorizzazione dell'INFN, e in conformità all'art. 105 del d.lgs. 50/2016, solo se lo avrà dichiarato in sede di offerta.

### 6. DIVIETO CESSIONE CONTRATTO:

E' fatto divieto all'Impresa di cedere, a qualsiasi titolo, il contratto, a pena di nullità della cessione medesima.

### 7. OBBLIGHI DELL'APPALTATORE:

L'Impresa si impegna ad ottemperare a tutti gli obblighi derivanti da disposizioni legislative e regolamentari vigenti in materia di retribuzione, previdenza e assistenza.

L'Impresa si obbliga, inoltre, all'osservanza delle norme in materia di sicurezza sul lavoro, ai sensi del d.lgs. n. 81/2008 e s.m.i. L'Impresa si obbliga, per quanto compatibile, a far osservare ai propri dipendenti e Collaboratori il Codice di comportamento in materia di anticorruzione del personale INFN, pubblicato nella sezione "Amministrazione trasparente" del sito istituzionale INFN. Nelle ipotesi di grave violazione delle disposizioni ivi contenute, l'INFN si riserva la facoltà di risolvere il contratto.

L'Impresa si obbliga al rispetto delle disposizioni di cui all'art. 53, comma 16-ter del d.lgs. n. 165/2001 e s.m.i. in materia di conferimento di incarichi o contratti di lavoro ad ex dipendenti INFN, pena l'obbligo di restituzione dei compensi illegittimamente percepiti ed accertati in esecuzione dell'affidamento.

### 8. VERIFICA DI CONFORMITA' / ATTESTAZIONE DI REGOLARE ESECUZIONE:

La verifica della conformità delle prestazioni eseguite a quelle pattuite sarà effettuata a cura del direttore dell'esecuzione del contratto, ai sensi del combinato disposto degli artt. 102, comma 2, del d.lgs. n. 50/2016 e art. 237 del d.P.R. n. 207/2010 entro 40 (quaranta) giorni dalla consegna della fornitura.

### 9. FATTURAZIONE E PAGAMENTI:



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Le fatture, da emettersi in formato elettronico, dovranno essere trasmesse tramite il sistema di Interscambio dell'Agenzia delle Entrate utilizzando il Codice Univoco Ufficio: **F2WDCT**

Il pagamento del corrispettivo sarà effettuato entro e non oltre 30 giorni dalla trasmissione della fattura da emettersi previa verifica di conformità da effettuarsi entro 40 (quaranta) giorni dalla consegna della fornitura, mediante bonifico su conto corrente dedicato del quale l'Impresa si obbliga a garantire la tracciabilità ai sensi della L. 136/2010 e s.m.i. La violazione di tale obbligo determina la risoluzione di diritto del contratto. Il pagamento sarà, inoltre, subordinato alla verifica della regolarità contributiva e fiscale dell'Impresa.

**10. RISOLUZIONE PER INADEMPIMENTO E RECESSO:**

Nel caso di inadempimento delle obbligazioni contrattuali l'INFN si riserva il diritto di risolvere il contratto ai sensi e per gli effetti dell'art. 1453 c.c., con comunicazione scritta da inviarsi con raccomandata a/r, con un preavviso di 20 (venti) giorni.

Restano in ogni caso impregiudicati i diritti dell'INFN al risarcimento di eventuali danni e all'incameramento della garanzia definitiva.

L'INFN si riserva, inoltre, il diritto di recedere unilateralmente dal contratto in qualsiasi momento senza alcun onere a suo carico, con un preavviso di almeno 20 (venti) giorni da comunicarsi all'Impresa mediante raccomandata a/r.

In caso di recesso all'Impresa spetterà il corrispettivo limitatamente alla prestazione eseguita e al decimo dell'importo delle forniture non eseguiti ai sensi dell'art. 109 del d.lgs. n. 50/2016, secondo i corrispettivi e le condizioni previsti nel contratto.

**11. GARANZIA:**

Per i beni oggetto del contratto, in base agli artt. 1490 e 1495 del c.c., l'appaltatore dovrà fornire idonea garanzia, non inferiore a 12 mesi.

**12. FORO COMPETENTE:**

Per eventuali controversie tra le Parti inerenti al Contratto, sarà competente in via esclusiva il Foro di Roma.

**13. TRATTAMENTO DEI DATI PERSONALI:**

I dati personali saranno raccolti e trattati unicamente per la gestione dell'attività di gara, ai sensi del d.lgs. n. 196/03 e s.m.i. Responsabile del trattamento dei dati: Direttore della Struttura INFN.

